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ELEN 511 - Advanced Computer Architecture

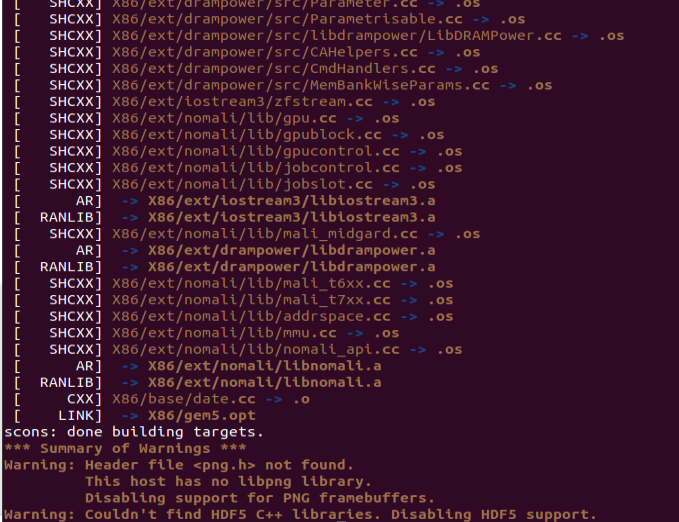
ASSIGNMENT #1 GEM 5

Prof. Hoeseok Yang

Santa Clara University

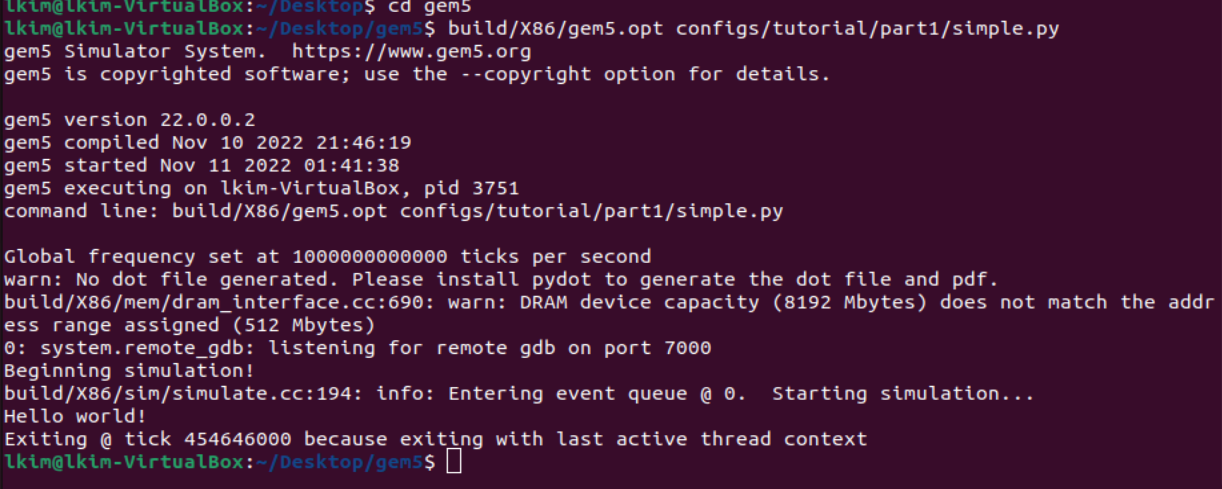
Fall Quarter 2022

**Homework #1**

**Part 0 - setup:**

I first started off by downloading virtualbox and had to build an image twice because the first one did not have enough disk drive to properly run Ubuntu and gem5. Furthermore, everything was fairly seamless other than the actual build command which required me to think outside the box and experiment with how to make scons work for my system. Ultimately, I was able to build gem5 as seen in the screenshot above.

**Part 1 - creating a simple configuration:**



This portion was fairly simple as the documentation was very procedural and was informative because it explained the purpose of each parameter that composed of our simple configuration.

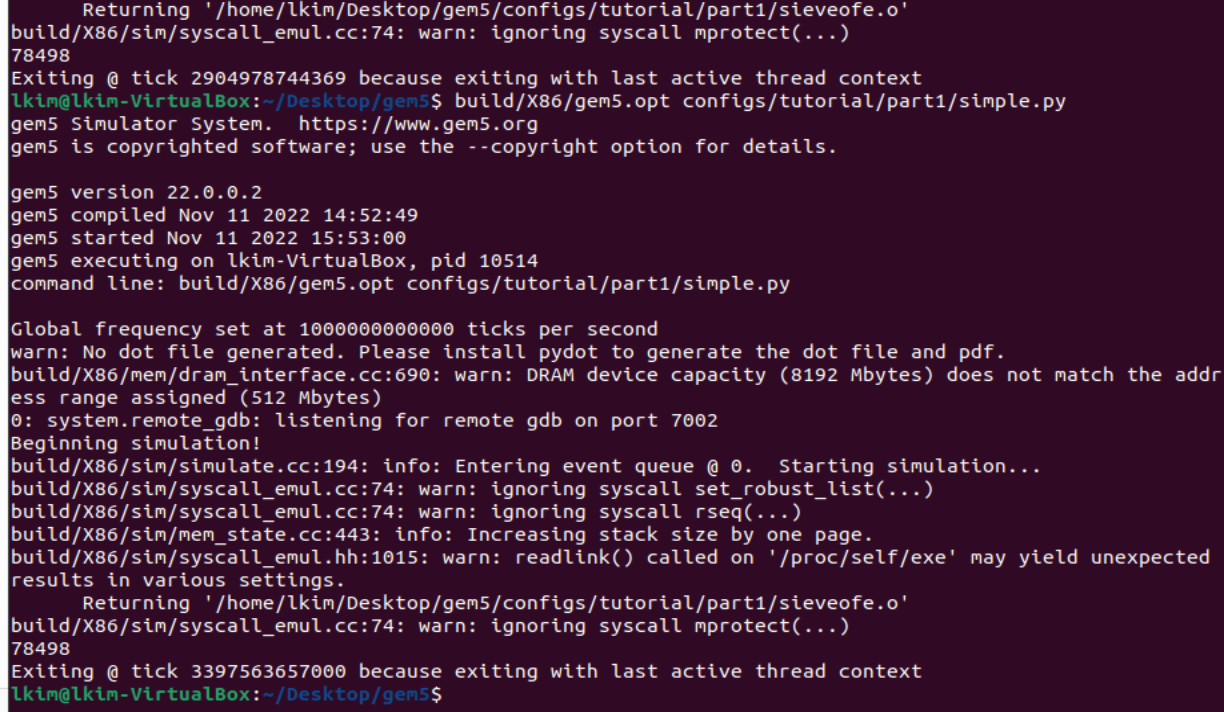
**Part 2 - Write and run your own test application:**

**Configuration 3:**

system.clk\_domain.clock = '1GHz'

system.cpu = TimingSimpleCPU()

system.mem\_ctrl.dram = DDR3\_1600\_8x8()



This portion of the assignment required me to understand how the algorithm which is called Shiva veritas the knees Works. After having done so I created a C program that takes a integer and I’ll puts the number of prime numbers from zero up to that and put it in a jar, implementing this portion of my own test application required me to understand the compilation of test applications, and end where it applies in comparison to the program in build.

**Part 3 - Analyze the statistics:**

The statistics show a plethora of relevant CPU statistics. And he statistics range from a number of arithmetic logic. Unit axis is whether those are for integers, floats, vectors. I was looking for relevant cash information, but was not able to find any. The closest thing to some resemblance of a cash was a TLB. there were statistics referring to the translation lookaside buffer, those being accesses/ misses on read/write requests.

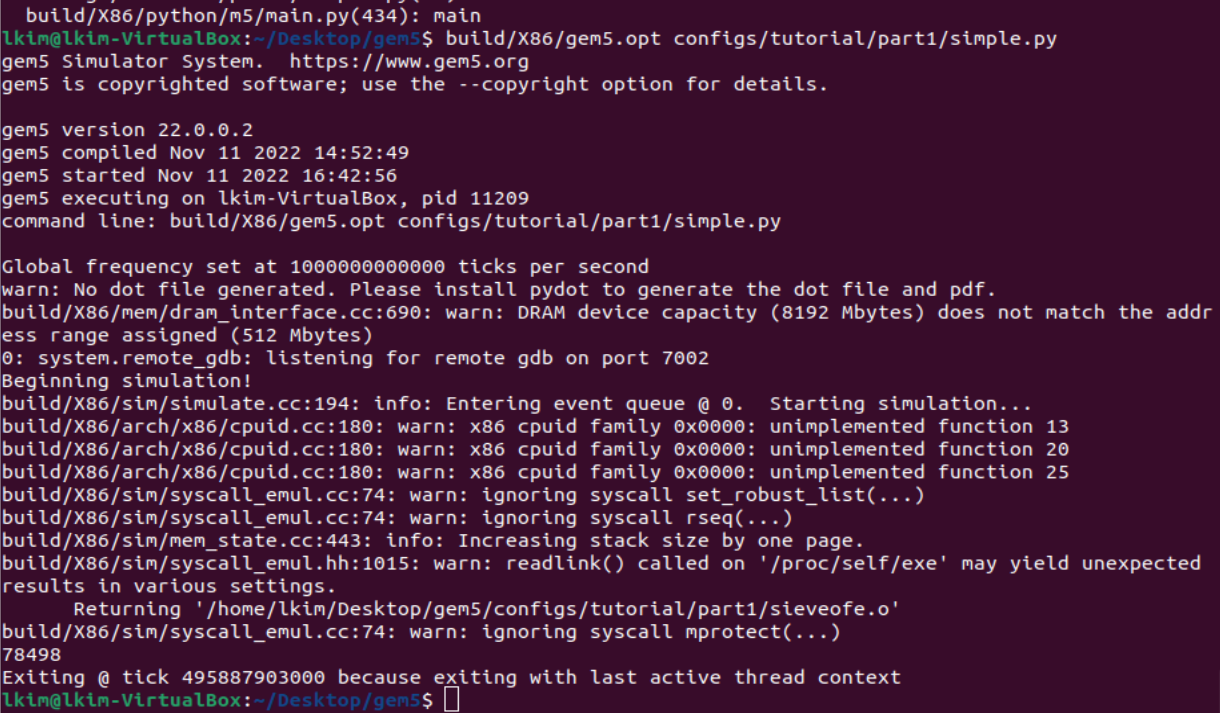
**Part 4 - Alternative Configurations:**

**Configuration 4.1:**

system.clk\_domain.clock = '1GHz'

system.cpu = X86O3CPU()

system.mem\_ctrl.dram = DDR3\_1600\_8x8()

We can expect a lot of changes and we did see many changes as the actual cpu was interchanged with a different processor. We can see that for this configuration the simulation time was MUCH faster. With a time of 0.49 from the last 3.39 seconds. This makes sense as when we pull up the tlb accesses, we can read,

system.cpu.mmu.itb.rdAccesses 0 # TLB accesses on read requests (Count)

system.cpu.mmu.itb.wrAccesses 6497328 # TLB accesses on write requests (Count)

system.cpu.mmu.itb.rdMisses 0 # TLB misses on read requests (Count)

system.cpu.mmu.itb.wrMisses 93 # TLB misses on write requests (Count

Versus the original

system.cpu.mmu.itb.rdAccesses 0 # TLB accesses on read requests (Count)

system.cpu.mmu.itb.wrAccesses 47529643 # TLB accesses on write requests (Count)

system.cpu.mmu.itb.rdMisses 0 # TLB misses on read requests (Count)

system.cpu.mmu.itb.wrMisses 56 # TLB misses on write requests (Count)

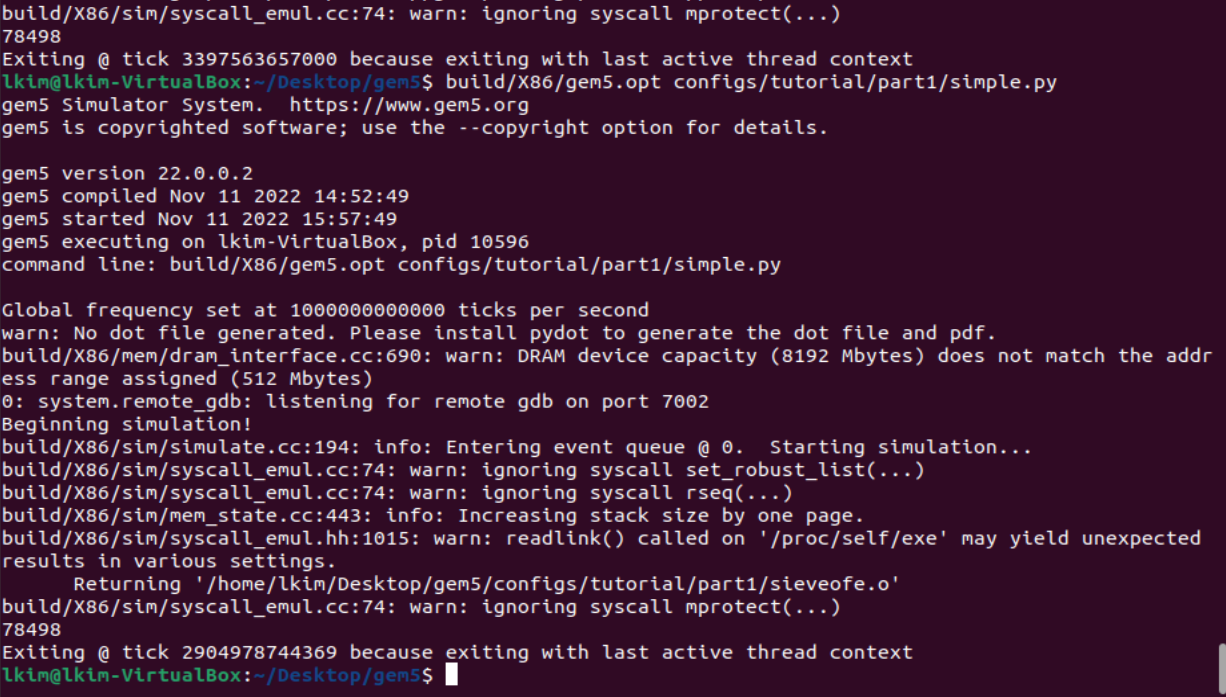
We observe that there is a huge difference is the number of accesses in the itb by almost a magnitude as there were 47.5 million accesses versus the new 6 million access reads. This could result in how the simulation time was also drastically reduced.

**Configuration 4.2:**

system.clk\_domain.clock = '3GHz'

system.cpu = TimingSimpleCPU()

system.mem\_ctrl.dram = DDR3\_1600\_8x8()



For this configuration, we have a difference in the clock speed that we are using. We were using 1GHz, but now we are using 3GHz.

The change int clock is confirmed in our statistics line that says   
system.clk\_domain.clock 333 # Clock period in ticks (Tick)

And it is shown as the frequency increased by threefold and the period was decreased by threefold by comparison.

The number of tlb accesses/misses on read/write requests stayed the same which is to be expected as there is no change in the processing other than the speed. Intuitively, we can see that the simulation time is faster from 3.39 to 2.90.

**Configuration 4.3:**

system.clk\_domain.clock = '1GHz'

system.cpu = TimingSimpleCPU()

system.mem\_ctrl.dram = DDR3\_2133\_8x8()



For this configuration, we have a difference in the memory that we are using. We were using DDR3\_1600\_8x8, but now we are using DDR3\_2133\_8x8.

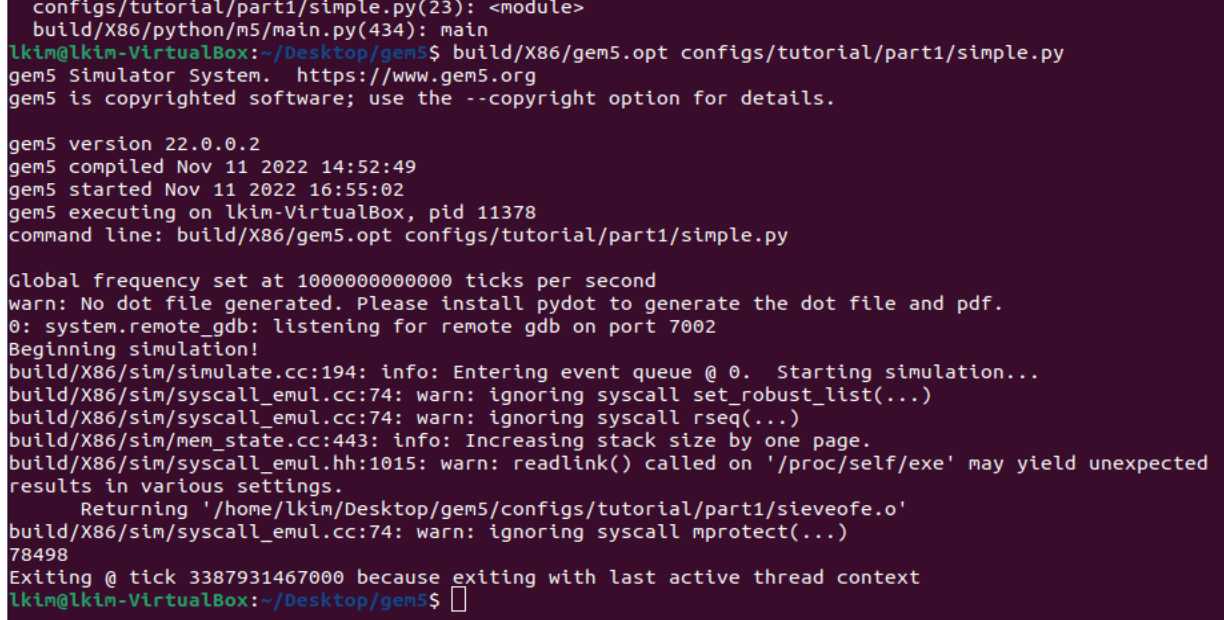
**Configuration 4.4:**

system.clk\_domain.clock = '1GHz'

system.cpu = TimingSimpleCPU()

system.mem\_ctrl.dram = LPDDR2\_S4\_1066\_1x32()

For this configuration, we have a difference in the memory that we are using. We were using DDR3\_1600\_8x8, but now we are using LPDDR2\_S4\_1066\_1x32(). I had to experiment a little bit with the sizing of the memory, but it does make sense that it turned out to be 1x32 as it is a low power memory which means that the bandwidth is likely to be much smaller.



**Stats 3**

---------- Begin Simulation Statistics ----------

simSeconds 3.397564 # Number of seconds simulated (Second)

simTicks 3397563657000 # Number of ticks simulated (Tick)

finalTick 3397563657000 # Number of ticks from beginning of simulation (restored from checkpoints and never reset) (Tick)

simFreq 1000000000000 # The number of ticks per simulated second ((Tick/Second))

hostSeconds 173.61 # Real time elapsed on the host (Second)

hostTickRate 19570292456 # The number of ticks simulated per host second (ticks/s) ((Tick/Second))

hostMemory 655500 # Number of bytes of host memory used (Byte)

simInsts 36199500 # Number of instructions simulated (Count)

simOps 76555494 # Number of ops (including micro ops) simulated (Count)

hostInstRate 208512 # Simulator instruction rate (inst/s) ((Count/Second))

hostOpRate 440967 # Simulator op (including micro ops) rate (op/s) ((Count/Second))

system.clk\_domain.clock 1000 # Clock period in ticks (Tick)

system.clk\_domain.voltage\_domain.voltage 1 # Voltage in Volts (Volt)

system.cpu.numCycles 3397563657 # Number of cpu cycles simulated (Cycle)

system.cpu.numWorkItemsStarted 0 # Number of work items this cpu started (Count)

system.cpu.numWorkItemsCompleted 0 # Number of work items this cpu completed (Count)

system.cpu.exec\_context.thread\_0.numInsts 36199500 # Number of instructions committed (Count)

system.cpu.exec\_context.thread\_0.numOps 76555494 # Number of ops (including micro ops) committed (Count)

system.cpu.exec\_context.thread\_0.numIntAluAccesses 76554574 # Number of integer alu accesses (Count)

system.cpu.exec\_context.thread\_0.numFpAluAccesses 1471 # Number of float alu accesses (Count)

system.cpu.exec\_context.thread\_0.numVecAluAccesses 0 # Number of vector alu accesses (Count)

system.cpu.exec\_context.thread\_0.numCallsReturns 373 # Number of times a function call or return occured (Count)

system.cpu.exec\_context.thread\_0.numCondCtrlInsts 5125826 # Number of instructions that are conditional controls (Count)

system.cpu.exec\_context.thread\_0.numIntInsts 76554574 # Number of integer instructions (Count)

system.cpu.exec\_context.thread\_0.numFpInsts 1471 # Number of float instructions (Count)

system.cpu.exec\_context.thread\_0.numVecInsts 0 # Number of vector instructions (Count)

system.cpu.exec\_context.thread\_0.numIntRegReads 87007781 # Number of times the integer registers were read (Count)

system.cpu.exec\_context.thread\_0.numIntRegWrites 58976338 # Number of times the integer registers were written (Count)

system.cpu.exec\_context.thread\_0.numFpRegReads 1590 # Number of times the floating registers were read (Count)

system.cpu.exec\_context.thread\_0.numFpRegWrites 859 # Number of times the floating registers were written (Count)

system.cpu.exec\_context.thread\_0.numVecRegReads 0 # Number of times the vector registers were read (Count)

system.cpu.exec\_context.thread\_0.numVecRegWrites 0 # Number of times the vector registers were written (Count)

system.cpu.exec\_context.thread\_0.numVecPredRegReads 0 # Number of times the predicate registers were read (Count)

system.cpu.exec\_context.thread\_0.numVecPredRegWrites 0 # Number of times the predicate registers were written (Count)

system.cpu.exec\_context.thread\_0.numCCRegReads 26632889 # Number of times the CC registers were read (Count)

system.cpu.exec\_context.thread\_0.numCCRegWrites 24904504 # Number of times the CC registers were written (Count)

system.cpu.exec\_context.thread\_0.numMiscRegReads 37276209 # Number of times the Misc registers were read (Count)

system.cpu.exec\_context.thread\_0.numMiscRegWrites 0 # Number of times the Misc registers were written (Count)

system.cpu.exec\_context.thread\_0.numMemRefs 22899889 # Number of memory refs (Count)

system.cpu.exec\_context.thread\_0.numLoadInsts 15574080 # Number of load instructions (Count)

system.cpu.exec\_context.thread\_0.numStoreInsts 7325809 # Number of store instructions (Count)

system.cpu.exec\_context.thread\_0.numIdleCycles 0.001000 # Number of idle cycles (Cycle)

system.cpu.exec\_context.thread\_0.numBusyCycles 3397563656.999000 # Number of busy cycles (Cycle)

system.cpu.exec\_context.thread\_0.notIdleFraction 1.000000 # Percentage of non-idle cycles (Ratio)

system.cpu.exec\_context.thread\_0.idleFraction 0.000000 # Percentage of idle cycles (Ratio)

system.cpu.exec\_context.thread\_0.numBranches 5126544 # Number of branches fetched (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::No\_OpClass 236 0.00% 0.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntAlu 53654589 70.09% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntMult 177 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntDiv 28 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatAdd 184 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatCvt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMisc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAdd 8 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAddAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAlu 98 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdCvt 54 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMisc 252 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShift 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShiftAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatCvt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMisc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatReduceAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatReduceCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAes 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAesMix 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha1Hash 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha1Hash2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha256Hash 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha256Hash2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShaSigma2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShaSigma3 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdPredAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::MemRead 15573939 20.34% 90.43% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::MemWrite 7325245 9.57% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMemRead 141 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMemWrite 564 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IprAccess 0 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::InstPrefetch 0 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::total 76555515 # Class of executed instruction. (Count)

system.cpu.interrupts.clk\_domain.clock 16000 # Clock period in ticks (Tick)

system.cpu.mmu.dtb.rdAccesses 15574084 # TLB accesses on read requests (Count)

system.cpu.mmu.dtb.wrAccesses 7325810 # TLB accesses on write requests (Count)

system.cpu.mmu.dtb.rdMisses 421 # TLB misses on read requests (Count)

system.cpu.mmu.dtb.wrMisses 28844 # TLB misses on write requests (Count)

system.cpu.mmu.dtb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 3397563657000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.mmu.itb.rdAccesses 0 # TLB accesses on read requests (Count)

system.cpu.mmu.itb.wrAccesses 47529643 # TLB accesses on write requests (Count)

system.cpu.mmu.itb.rdMisses 0 # TLB misses on read requests (Count)

system.cpu.mmu.itb.wrMisses 56 # TLB misses on write requests (Count)

system.cpu.mmu.itb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 3397563657000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.power\_state.pwrStateResidencyTicks::ON 3397563657000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.thread\_0.numInsts 0 # Number of Instructions committed (Count)

system.cpu.thread\_0.numOps 0 # Number of Ops committed (Count)

system.cpu.thread\_0.numMemRefs 0 # Number of Memory References (Count)

system.cpu.workload.numSyscalls 17 # Number of system calls (Count)

system.mem\_ctrl.avgPriority\_cpu.inst::samples 47529643.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.avgPriority\_cpu.data::samples 6934363.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.priorityMinLatency 0.000000018750 # per QoS priority minimum request to response latency (Second)

system.mem\_ctrl.priorityMaxLatency 2.262941650750 # per QoS priority maximum request to response latency (Second)

system.mem\_ctrl.numReadWriteTurnArounds 44356 # Number of turnarounds from READ to WRITE (Count)

system.mem\_ctrl.numWriteReadTurnArounds 44356 # Number of turnarounds from WRITE to READ (Count)

system.mem\_ctrl.numStayReadState 115662297 # Number of times bus staying in READ state (Count)

system.mem\_ctrl.numStayWriteState 665707 # Number of times bus staying in WRITE state (Count)

system.mem\_ctrl.readReqs 63103726 # Number of read requests accepted (Count)

system.mem\_ctrl.writeReqs 7325807 # Number of write requests accepted (Count)

system.mem\_ctrl.readBursts 63103726 # Number of controller read bursts, including those serviced by the write queue (Count)

system.mem\_ctrl.writeBursts 7325807 # Number of controller write bursts, including those merged in the write queue (Count)

system.mem\_ctrl.servicedByWrQ 9349484 # Number of controller read bursts serviced by the write queue (Count)

system.mem\_ctrl.mergedWrBursts 6616043 # Number of controller write bursts merged with an existing one (Count)

system.mem\_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write (Count)

system.mem\_ctrl.avgRdQLen 1.00 # Average read queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.avgWrQLen 24.98 # Average write queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.numRdRetry 0 # Number of times read queue was full causing retry (Count)

system.mem\_ctrl.numWrRetry 0 # Number of times write queue was full causing retry (Count)

system.mem\_ctrl.readPktSize::0 1001231 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::1 19 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::2 14571441 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::3 47531035 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::4 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::5 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::6 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::0 3122099 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::1 3 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::2 4201939 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::3 1766 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::4 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::5 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::6 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.rdQLenPdf::0 53754238 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::1 4 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::2 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::3 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::4 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::5 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::6 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::7 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::8 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::9 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::10 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::11 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::12 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::13 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::14 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::15 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::16 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::17 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::18 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::0 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::1 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::2 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::3 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::4 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::5 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::6 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::7 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::8 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::9 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::10 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::11 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::12 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::13 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::14 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::15 24 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::16 24 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::17 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::18 44357 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::19 44357 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::20 44357 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::21 44357 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::22 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::23 44357 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::24 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::25 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::26 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::27 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::28 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::29 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::30 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::31 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::32 44356 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::34 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::35 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::50 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::51 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::53 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::54 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::55 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.rdPerTurnAround::samples 44356 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::mean 1211.878664 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::gmean 338.313167 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::stdev 86600.937407 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::0-1.04858e+06 44355 100.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::1.78258e+07-1.88744e+07 1 0.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::total 44356 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.wrPerTurnAround::samples 44356 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::mean 16.001037 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::gmean 16.000977 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::stdev 0.045531 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::16 44333 99.95% 99.95% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::18 23 0.05% 100.00% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::total 44356 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.bytesReadWrQ 598366976 # Total number of bytes read from write queue (Byte)

system.mem\_ctrl.bytesReadSys 439535306 # Total read bytes from the system interface side (Byte)

system.mem\_ctrl.bytesWrittenSys 19943987 # Total written bytes from the system interface side (Byte)

system.mem\_ctrl.avgRdBWSys 129367791.26843597 # Average system read bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.avgWrBWSys 5870084.86475578 # Average system write bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.totGap 3397563531000 # Total gap between requests (Tick)

system.mem\_ctrl.avgGap 48240.61 # Average gap between requests ((Tick/Count))

system.mem\_ctrl.requestorReadBytes::cpu.inst 380237144 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorReadBytes::cpu.data 21899389 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorWriteBytes::cpu.data 720805 # Per-requestor bytes write to memory (Byte)

system.mem\_ctrl.requestorReadRate::cpu.inst 111914648.962234288454 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadRate::cpu.data 6445615.508889934048 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorWriteRate::cpu.data 212153.493729227281 # Per-requestor bytes write to memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadAccesses::cpu.inst 47529643 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorReadAccesses::cpu.data 15574083 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorWriteAccesses::cpu.data 7325807 # Per-requestor write serviced memory accesses (Count)

system.mem\_ctrl.requestorReadTotalLat::cpu.inst 1154721525250 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorReadTotalLat::cpu.data 270488760000 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorWriteTotalLat::cpu.data 78277683342750 # Per-requestor write total memory access latency (Tick)

system.mem\_ctrl.requestorReadAvgLat::cpu.inst 24294.77 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorReadAvgLat::cpu.data 17367.88 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorWriteAvgLat::cpu.data 10685195.96 # Per-requestor write average memory access latency ((Tick/Count))

system.mem\_ctrl.dram.bytesRead::cpu.inst 380237144 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::cpu.data 59298162 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::total 439535306 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::cpu.inst 380237144 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::total 380237144 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::cpu.data 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::total 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.numReads::cpu.inst 47529643 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::cpu.data 15574083 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::total 63103726 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::cpu.data 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::total 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.bwRead::cpu.inst 111914649 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::cpu.data 17453142 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::total 129367791 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::cpu.inst 111914649 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::total 111914649 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::cpu.data 5870085 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::total 5870085 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.inst 111914649 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.data 23323227 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::total 135237876 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.readBursts 53754242 # Number of DRAM read bursts (Count)

system.mem\_ctrl.dram.writeBursts 709742 # Number of DRAM write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::0 52796429 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::1 58693 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::2 58164 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::3 61969 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::4 66160 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::5 66349 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::6 65557 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::7 66179 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::8 65688 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::9 67381 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::10 66785 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::11 65843 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::12 66137 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::13 62864 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::14 58980 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::15 61064 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::0 44249 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::1 41967 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::2 41529 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::3 42110 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::4 44344 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::5 45114 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::6 45485 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::7 45865 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::8 46100 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::9 46302 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::10 46512 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::11 46705 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::12 46857 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::13 44923 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::14 40793 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::15 40887 # Per bank write bursts (Count)

system.mem\_ctrl.dram.totQLat 417318247750 # Total ticks spent queuing (Tick)

system.mem\_ctrl.dram.totBusLat 268771210000 # Total ticks spent in databus transfers (Tick)

system.mem\_ctrl.dram.totMemAccLat 1425210285250 # Total ticks spent from burst creation until serviced by the DRAM (Tick)

system.mem\_ctrl.dram.avgQLat 7763.45 # Average queueing delay per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgBusLat 5000.00 # Average bus latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgMemAccLat 26513.45 # Average memory access latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.readRowHits 42118516 # Number of row buffer hits during reads (Count)

system.mem\_ctrl.dram.writeRowHits 648898 # Number of row buffer hits during writes (Count)

system.mem\_ctrl.dram.readRowHitRate 78.35 # Row buffer hit rate for reads (Ratio)

system.mem\_ctrl.dram.writeRowHitRate 91.43 # Row buffer hit rate for writes (Ratio)

system.mem\_ctrl.dram.bytesPerActivate::samples 11696565 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::mean 298.009921 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::gmean 169.664060 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::stdev 304.957490 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::0-127 5505879 47.07% 47.07% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::128-255 2141340 18.31% 65.38% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::256-383 125989 1.08% 66.46% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::384-511 285359 2.44% 68.90% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::512-639 922086 7.88% 76.78% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::640-767 2040896 17.45% 94.23% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::768-895 38479 0.33% 94.56% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::896-1023 47645 0.41% 94.97% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::1024-1151 588892 5.03% 100.00% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::total 11696565 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesRead 3440271488 # Total bytes read (Byte)

system.mem\_ctrl.dram.bytesWritten 45423488 # Total bytes written (Byte)

system.mem\_ctrl.dram.avgRdBW 1012.570134 # Average DRAM read bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.avgWrBW 13.369430 # Average DRAM write bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s ((Byte/Second))

system.mem\_ctrl.dram.busUtil 8.02 # Data bus utilization in percentage (Ratio)

system.mem\_ctrl.dram.busUtilRead 7.91 # Data bus utilization in percentage for reads (Ratio)

system.mem\_ctrl.dram.busUtilWrite 0.10 # Data bus utilization in percentage for writes (Ratio)

system.mem\_ctrl.dram.pageHitRate 78.52 # Row buffer hit rate, read and write combined (Ratio)

system.mem\_ctrl.dram.power\_state.pwrStateResidencyTicks::UNDEFINED 3397563657000 # Cumulative time (in ticks) in various power states (Tick)

system.mem\_ctrl.dram.rank0.actEnergy 82778475360 # Energy for activate commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preEnergy 43997787900 # Energy for precharge commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.readEnergy 380130030000 # Energy for read commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.writeEnergy 1830460860 # Energy for write commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.refreshEnergy 268200622560.000031 # Energy for refresh commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actBackEnergy 1480927690350 # Energy for active background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preBackEnergy 57567442080 # Energy for precharge background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.totalEnergy 2315432509110 # Total energy per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.averagePower 681.497903 # Core power per rank (mW) (Watt)

system.mem\_ctrl.dram.rank0.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::IDLE 21716258750 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::REF 113452040000 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::SREF 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::PRE\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT 3262395358250 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.actEnergy 735034440 # Energy for activate commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.preEnergy 390676275 # Energy for precharge commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.readEnergy 3675257880 # Energy for read commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.writeEnergy 1874392380 # Energy for write commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.refreshEnergy 268200622560.000031 # Energy for refresh commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.actBackEnergy 295943547990 # Energy for active background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.preBackEnergy 1055448825120 # Energy for precharge background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.totalEnergy 1626268356645 # Total energy per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.averagePower 478.657215 # Core power per rank (mW) (Watt)

system.mem\_ctrl.dram.rank1.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::IDLE 2741190158500 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::REF 113452040000 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::SREF 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::PRE\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::ACT 542921458500 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::ACT\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.power\_state.pwrStateResidencyTicks::UNDEFINED 3397563657000 # Cumulative time (in ticks) in various power states (Tick)

system.membus.transDist::ReadReq 63103710 # Transaction distribution (Count)

system.membus.transDist::ReadResp 63103710 # Transaction distribution (Count)

system.membus.transDist::WriteReq 7325791 # Transaction distribution (Count)

system.membus.transDist::WriteResp 7325791 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadResp 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteResp 16 # Transaction distribution (Count)

system.membus.pktCount\_system.cpu.icache\_port::system.mem\_ctrl.port 95059286 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.icache\_port::total 95059286 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::system.mem\_ctrl.port 45799780 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::total 45799780 # Packet count per connected requestor and responder (Count)

system.membus.pktCount::total 140859066 # Packet count per connected requestor and responder (Count)

system.membus.pktSize\_system.cpu.icache\_port::system.mem\_ctrl.port 380237144 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.icache\_port::total 380237144 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::system.mem\_ctrl.port 79242149 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::total 79242149 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize::total 459479293 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.snoops 0 # Total snoops (Count)

system.membus.snoopTraffic 0 # Total snoop traffic (Byte)

system.membus.snoopFanout::samples 70429533 # Request fanout histogram (Count)

system.membus.snoopFanout::mean 0 # Request fanout histogram (Count)

system.membus.snoopFanout::stdev 0 # Request fanout histogram (Count)

system.membus.snoopFanout::underflows 0 0.00% 0.00% # Request fanout histogram (Count)

system.membus.snoopFanout::0 70429533 100.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::1 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::overflows 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::min\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::max\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::total 70429533 # Request fanout histogram (Count)

system.membus.power\_state.pwrStateResidencyTicks::UNDEFINED 3397563657000 # Cumulative time (in ticks) in various power states (Tick)

system.membus.reqLayer2.occupancy 77755340000 # Layer occupancy (ticks) (Tick)

system.membus.reqLayer2.utilization 0.0 # Layer utilization (Ratio)

system.membus.respLayer0.occupancy 109734297750 # Layer occupancy (ticks) (Tick)

system.membus.respLayer0.utilization 0.0 # Layer utilization (Ratio)

system.membus.respLayer1.occupancy 42693685000 # Layer occupancy (ticks) (Tick)

system.membus.respLayer1.utilization 0.0 # Layer utilization (Ratio)

system.membus.snoop\_filter.totRequests 0 # Total number of requests made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleRequests 0 # Number of requests hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiRequests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.membus.snoop\_filter.totSnoops 0 # Total number of snoops made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleSnoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiSnoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.workload.inst.arm 0 # number of arm instructions executed (Count)

system.workload.inst.quiesce 0 # number of quiesce instructions executed (Count)

---------- End Simulation Statistics ----------

**Stats 4.1**

---------- Begin Simulation Statistics ----------

simSeconds 0.495888 # Number of seconds simulated (Second)

simTicks 495887903000 # Number of ticks simulated (Tick)

finalTick 495887903000 # Number of ticks from beginning of simulation (restored from checkpoints and never reset) (Tick)

simFreq 1000000000000 # The number of ticks per simulated second ((Tick/Second))

hostSeconds 410.22 # Real time elapsed on the host (Second)

hostTickRate 1208826443 # The number of ticks simulated per host second (ticks/s) ((Tick/Second))

hostMemory 658572 # Number of bytes of host memory used (Byte)

simInsts 36199500 # Number of instructions simulated (Count)

simOps 76555494 # Number of ops (including micro ops) simulated (Count)

hostInstRate 88244 # Simulator instruction rate (inst/s) ((Count/Second))

hostOpRate 186619 # Simulator op (including micro ops) rate (op/s) ((Count/Second))

system.clk\_domain.clock 1000 # Clock period in ticks (Tick)

system.clk\_domain.voltage\_domain.voltage 1 # Voltage in Volts (Volt)

system.cpu.numCycles 495887904 # Number of cpu cycles simulated (Cycle)

system.cpu.numWorkItemsStarted 0 # Number of work items this cpu started (Count)

system.cpu.numWorkItemsCompleted 0 # Number of work items this cpu completed (Count)

system.cpu.instsAdded 77908802 # Number of instructions added to the IQ (excludes non-spec) (Count)

system.cpu.nonSpecInstsAdded 100 # Number of non-speculative instructions added to the IQ (Count)

system.cpu.instsIssued 79441802 # Number of instructions issued (Count)

system.cpu.squashedInstsIssued 60 # Number of squashed instructions issued (Count)

system.cpu.squashedInstsExamined 1353402 # Number of squashed instructions iterated over during squash; mainly for profiling (Count)

system.cpu.squashedOperandsExamined 3637174 # Number of squashed operands that are examined and possibly removed from graph (Count)

system.cpu.squashedNonSpecRemoved 52 # Number of squashed non-spec instructions that were removed (Count)

system.cpu.numIssuedDist::samples 302528199 # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::mean 0.262593 # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::stdev 0.775607 # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::underflows 0 0.00% 0.00% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::0 261961260 86.59% 86.59% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::1 17194560 5.68% 92.27% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::2 13725745 4.54% 96.81% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::3 4968416 1.64% 98.45% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::4 3794029 1.25% 99.71% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::5 591194 0.20% 99.90% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::6 292661 0.10% 100.00% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::7 220 0.00% 100.00% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::8 114 0.00% 100.00% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::overflows 0 0.00% 100.00% # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::min\_value 0 # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::max\_value 8 # Number of insts issued each cycle (Count)

system.cpu.numIssuedDist::total 302528199 # Number of insts issued each cycle (Count)

system.cpu.statFuBusy::No\_OpClass 0 0.00% 0.00% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::IntAlu 103 51.50% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::IntMult 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::IntDiv 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatAdd 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatCmp 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatCvt 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatMult 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatMultAcc 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatDiv 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatMisc 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatSqrt 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdAdd 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdAddAcc 0 0.00% 51.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdAlu 8 4.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdCmp 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdCvt 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdMisc 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdMult 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdMultAcc 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdShift 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdShiftAcc 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdDiv 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdSqrt 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatAdd 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatAlu 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatCmp 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatCvt 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatDiv 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatMisc 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatMult 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatMultAcc 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatSqrt 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdReduceAdd 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdReduceAlu 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdReduceCmp 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatReduceAdd 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdFloatReduceCmp 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdAes 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdAesMix 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdSha1Hash 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdSha1Hash2 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdSha256Hash 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdSha256Hash2 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdShaSigma2 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdShaSigma3 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::SimdPredAlu 0 0.00% 55.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::MemRead 36 18.00% 73.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::MemWrite 12 6.00% 79.50% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatMemRead 27 13.50% 93.00% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::FloatMemWrite 14 7.00% 100.00% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::IprAccess 0 0.00% 100.00% # attempts to use FU when none available (Count)

system.cpu.statFuBusy::InstPrefetch 0 0.00% 100.00% # attempts to use FU when none available (Count)

system.cpu.statIssuedInstType\_0::No\_OpClass 486 0.00% 0.00% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::IntAlu 54244857 68.28% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::IntMult 203 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::IntDiv 28 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatAdd 211 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatCmp 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatCvt 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatMult 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatMultAcc 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatDiv 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatMisc 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatSqrt 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdAdd 8 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdAddAcc 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdAlu 142 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdCmp 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdCvt 54 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdMisc 256 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdMult 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdMultAcc 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdShift 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdShiftAcc 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdDiv 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdSqrt 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatAdd 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatAlu 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatCmp 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatCvt 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatDiv 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatMisc 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatMult 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatMultAcc 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatSqrt 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdReduceAdd 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdReduceAlu 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdReduceCmp 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatReduceAdd 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdFloatReduceCmp 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdAes 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdAesMix 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdSha1Hash 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdSha1Hash2 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdSha256Hash 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdSha256Hash2 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdShaSigma2 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdShaSigma3 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::SimdPredAlu 0 0.00% 68.28% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::MemRead 17868533 22.49% 90.78% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::MemWrite 7325835 9.22% 100.00% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatMemRead 531 0.00% 100.00% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::FloatMemWrite 658 0.00% 100.00% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::IprAccess 0 0.00% 100.00% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::InstPrefetch 0 0.00% 100.00% # Number of instructions issued per FU type, per thread (Count)

system.cpu.statIssuedInstType\_0::total 79441802 # Number of instructions issued per FU type, per thread (Count)

system.cpu.issueRate 0.160201 # Inst issue rate ((Count/Cycle))

system.cpu.fuBusy 200 # FU busy when requested (Count)

system.cpu.fuBusyRate 0.000003 # FU busy rate (busy events/executed inst) ((Count/Count))

system.cpu.intInstQueueReads 461407937 # Number of integer instruction queue reads (Count)

system.cpu.intInstQueueWrites 79260198 # Number of integer instruction queue writes (Count)

system.cpu.intInstQueueWakeupAccesses 77145937 # Number of integer instruction queue wakeup accesses (Count)

system.cpu.fpInstQueueReads 4126 # Number of floating instruction queue reads (Count)

system.cpu.fpInstQueueWrites 2208 # Number of floating instruction queue writes (Count)

system.cpu.fpInstQueueWakeupAccesses 1635 # Number of floating instruction queue wakeup accesses (Count)

system.cpu.vecInstQueueReads 0 # Number of vector instruction queue reads (Count)

system.cpu.vecInstQueueWrites 0 # Number of vector instruction queue writes (Count)

system.cpu.vecInstQueueWakeupAccesses 0 # Number of vector instruction queue wakeup accesses (Count)

system.cpu.intAluAccesses 79439434 # Number of integer alu accesses (Count)

system.cpu.fpAluAccesses 2082 # Number of floating point alu accesses (Count)

system.cpu.vecAluAccesses 0 # Number of vector alu accesses (Count)

system.cpu.numInsts 79441607 # Number of executed instructions (Count)

system.cpu.numLoadInsts 17868994 # Number of load instructions executed (Count)

system.cpu.numSquashedInsts 195 # Number of squashed instructions skipped in execute (Count)

system.cpu.numSwp 0 # Number of swp insts executed (Count)

system.cpu.numNop 0 # Number of nop insts executed (Count)

system.cpu.numRefs 25195469 # Number of memory reference insts executed (Count)

system.cpu.numBranches 5127301 # Number of branches executed (Count)

system.cpu.numStoreInsts 7326475 # Number of stores executed (Count)

system.cpu.numRate 0.160201 # Inst execution rate ((Count/Cycle))

system.cpu.timesIdled 14975769 # Number of times that the entire CPU went into an idle state and unscheduled itself (Count)

system.cpu.idleCycles 193359705 # Total number of cycles that the CPU has spent unscheduled due to idling (Cycle)

system.cpu.committedInsts 36199500 # Number of Instructions Simulated (Count)

system.cpu.committedOps 76555494 # Number of Ops (including micro ops) Simulated (Count)

system.cpu.cpi 13.698750 # CPI: Cycles Per Instruction ((Cycle/Count))

system.cpu.totalCpi 13.698750 # CPI: Total CPI of All Threads ((Cycle/Count))

system.cpu.ipc 0.072999 # IPC: Instructions Per Cycle ((Count/Cycle))

system.cpu.totalIpc 0.072999 # IPC: Total IPC of All Threads ((Count/Cycle))

system.cpu.intRegfileReads 89555031 # Number of integer regfile reads (Count)

system.cpu.intRegfileWrites 59566193 # Number of integer regfile writes (Count)

system.cpu.fpRegfileReads 1776 # Number of floating regfile reads (Count)

system.cpu.fpRegfileWrites 940 # Number of floating regfile writes (Count)

system.cpu.ccRegfileReads 26635654 # number of cc regfile reads (Count)

system.cpu.ccRegfileWrites 24907543 # number of cc regfile writes (Count)

system.cpu.miscRegfileReads 39739173 # number of misc regfile reads (Count)

system.cpu.MemDepUnit\_\_0.insertedLoads 15828722 # Number of loads inserted to the mem dependence unit. (Count)

system.cpu.MemDepUnit\_\_0.insertedStores 7414545 # Number of stores inserted to the mem dependence unit. (Count)

system.cpu.MemDepUnit\_\_0.conflictingLoads 6659652 # Number of conflicting loads. (Count)

system.cpu.MemDepUnit\_\_0.conflictingStores 162186 # Number of conflicting stores. (Count)

system.cpu.MemDepUnit\_\_1.insertedLoads 0 # Number of loads inserted to the mem dependence unit. (Count)

system.cpu.MemDepUnit\_\_1.insertedStores 0 # Number of stores inserted to the mem dependence unit. (Count)

system.cpu.MemDepUnit\_\_1.conflictingLoads 0 # Number of conflicting loads. (Count)

system.cpu.MemDepUnit\_\_1.conflictingStores 0 # Number of conflicting stores. (Count)

system.cpu.MemDepUnit\_\_2.insertedLoads 0 # Number of loads inserted to the mem dependence unit. (Count)

system.cpu.MemDepUnit\_\_2.insertedStores 0 # Number of stores inserted to the mem dependence unit. (Count)

system.cpu.MemDepUnit\_\_2.conflictingLoads 0 # Number of conflicting loads. (Count)

system.cpu.MemDepUnit\_\_2.conflictingStores 0 # Number of conflicting stores. (Count)

system.cpu.MemDepUnit\_\_3.insertedLoads 0 # Number of loads inserted to the mem dependence unit. (Count)

system.cpu.MemDepUnit\_\_3.insertedStores 0 # Number of stores inserted to the mem dependence unit. (Count)

system.cpu.MemDepUnit\_\_3.conflictingLoads 0 # Number of conflicting loads. (Count)

system.cpu.MemDepUnit\_\_3.conflictingStores 0 # Number of conflicting stores. (Count)

system.cpu.branchPred.lookups 5210998 # Number of BP lookups (Count)

system.cpu.branchPred.condPredicted 5209752 # Number of conditional branches predicted (Count)

system.cpu.branchPred.condIncorrect 83692 # Number of conditional branches incorrect (Count)

system.cpu.branchPred.BTBLookups 5202788 # Number of BTB lookups (Count)

system.cpu.branchPred.BTBHits 5201923 # Number of BTB hits (Count)

system.cpu.branchPred.BTBHitRatio 0.999834 # BTB Hit Ratio (Ratio)

system.cpu.branchPred.RASUsed 304 # Number of times the RAS was used to get a target. (Count)

system.cpu.branchPred.RASIncorrect 0 # Number of incorrect RAS predictions. (Count)

system.cpu.branchPred.indirectLookups 201 # Number of indirect predictor lookups. (Count)

system.cpu.branchPred.indirectHits 20 # Number of indirect target hits. (Count)

system.cpu.branchPred.indirectMisses 181 # Number of indirect misses. (Count)

system.cpu.branchPred.indirectMispredicted 96 # Number of mispredicted indirect branches. (Count)

system.cpu.commit.commitSquashedInsts 1353384 # The number of squashed insts skipped by commit (Count)

system.cpu.commit.commitNonSpecStalls 48 # The number of times commit has been forced to stall to communicate backwards (Count)

system.cpu.commit.branchMispredicts 83424 # The number of times a branch was mispredicted (Count)

system.cpu.commit.numCommittedDist::samples 302355604 # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::mean 0.253197 # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::stdev 0.930143 # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::underflows 0 0.00% 0.00% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::0 267859630 88.59% 88.59% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::1 16579102 5.48% 94.07% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::2 8666013 2.87% 96.94% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::3 4963209 1.64% 98.58% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::4 667693 0.22% 98.80% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::5 360 0.00% 98.80% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::6 416008 0.14% 98.94% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::7 3042593 1.01% 99.95% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::8 160996 0.05% 100.00% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::overflows 0 0.00% 100.00% # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::min\_value 0 # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::max\_value 8 # Number of insts commited each cycle (Count)

system.cpu.commit.numCommittedDist::total 302355604 # Number of insts commited each cycle (Count)

system.cpu.commit.instsCommitted 36199500 # Number of instructions committed (Count)

system.cpu.commit.opsCommitted 76555494 # Number of ops (including micro ops) committed (Count)

system.cpu.commit.memRefs 22899885 # Number of memory references committed (Count)

system.cpu.commit.loads 15574079 # Number of loads committed (Count)

system.cpu.commit.amos 0 # Number of atomic instructions committed (Count)

system.cpu.commit.membars 32 # Number of memory barriers committed (Count)

system.cpu.commit.branches 5126544 # Number of branches committed (Count)

system.cpu.commit.vectorInstructions 0 # Number of committed Vector instructions. (Count)

system.cpu.commit.floating 1470 # Number of committed floating point instructions. (Count)

system.cpu.commit.integer 76554570 # Number of committed integer instructions. (Count)

system.cpu.commit.functionCalls 189 # Number of function calls committed. (Count)

system.cpu.commit.committedInstType\_0::No\_OpClass 236 0.00% 0.00% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::IntAlu 53654572 70.09% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::IntMult 177 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::IntDiv 28 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatAdd 184 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatCmp 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatCvt 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatMult 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatMultAcc 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatDiv 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatMisc 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatSqrt 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdAdd 8 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdAddAcc 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdAlu 98 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdCmp 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdCvt 54 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdMisc 252 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdMult 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdMultAcc 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdShift 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdShiftAcc 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdDiv 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdSqrt 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatAdd 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatAlu 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatCmp 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatCvt 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatDiv 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatMisc 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatMult 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatMultAcc 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatSqrt 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdReduceAdd 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdReduceAlu 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdReduceCmp 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatReduceAdd 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdFloatReduceCmp 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdAes 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdAesMix 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdSha1Hash 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdSha1Hash2 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdSha256Hash 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdSha256Hash2 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdShaSigma2 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdShaSigma3 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::SimdPredAlu 0 0.00% 70.09% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::MemRead 15573938 20.34% 90.43% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::MemWrite 7325243 9.57% 100.00% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatMemRead 141 0.00% 100.00% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::FloatMemWrite 563 0.00% 100.00% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::IprAccess 0 0.00% 100.00% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction (Count)

system.cpu.commit.committedInstType\_0::total 76555494 # Class of committed instruction (Count)

system.cpu.commit.commitEligibleSamples 160996 # number cycles where commit BW limit reached (Cycle)

system.cpu.decode.idleCycles 250395229 # Number of cycles decode is idle (Cycle)

system.cpu.decode.blockedCycles 39425743 # Number of cycles decode is blocked (Cycle)

system.cpu.decode.runCycles 10623535 # Number of cycles decode is running (Cycle)

system.cpu.decode.unblockCycles 2000145 # Number of cycles decode is unblocking (Cycle)

system.cpu.decode.squashCycles 83547 # Number of cycles decode is squashing (Cycle)

system.cpu.decode.branchResolved 5202158 # Number of times decode resolved a branch (Count)

system.cpu.decode.branchMispred 288 # Number of times decode detected a branch misprediction (Count)

system.cpu.decode.decodedInsts 77909374 # Number of instructions handled by decode (Count)

system.cpu.decode.squashedInsts 1460 # Number of squashed instructions handled by decode (Count)

system.cpu.fetch.icacheStallCycles 249817678 # Number of cycles fetch is stalled on an Icache miss (Cycle)

system.cpu.fetch.insts 36790390 # Number of instructions fetch has processed (Count)

system.cpu.fetch.branches 5210998 # Number of branches that fetch encountered (Count)

system.cpu.fetch.predictedBranches 5202247 # Number of branches that fetch has predicted taken (Count)

system.cpu.fetch.cycles 52626470 # Number of cycles fetch has run and was not squashing or blocked (Cycle)

system.cpu.fetch.squashCycles 167670 # Number of cycles fetch has spent squashing (Cycle)

system.cpu.fetch.miscStallCycles 48 # Number of cycles fetch has spent waiting on interrupts, or bad addresses, or out of MSHRs (Cycle)

system.cpu.fetch.pendingTrapStallCycles 166 # Number of stall cycles due to pending traps (Cycle)

system.cpu.fetch.icacheWaitRetryStallCycles 2 # Number of stall cycles due to full MSHR (Cycle)

system.cpu.fetch.cacheLines 6497296 # Number of cache lines fetched (Count)

system.cpu.fetch.icacheSquashes 83630 # Number of outstanding Icache misses that were squashed (Count)

system.cpu.fetch.nisnDist::samples 302528199 # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::mean 0.257537 # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::stdev 1.293057 # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::underflows 0 0.00% 0.00% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::0 289904405 95.83% 95.83% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::1 265 0.00% 95.83% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::2 1000352 0.33% 96.16% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::3 308 0.00% 96.16% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::4 2129756 0.70% 96.86% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::5 304 0.00% 96.86% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::6 4276129 1.41% 98.28% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::7 329 0.00% 98.28% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::8 5216351 1.72% 100.00% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::overflows 0 0.00% 100.00% # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::min\_value 0 # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::max\_value 8 # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.nisnDist::total 302528199 # Number of instructions fetched each cycle (Total) (Count)

system.cpu.fetch.branchRate 0.010508 # Number of branch fetches per cycle (Ratio)

system.cpu.fetch.rate 0.074191 # Number of inst fetches per cycle ((Count/Cycle))

system.cpu.iew.idleCycles 0 # Number of cycles IEW is idle (Cycle)

system.cpu.iew.squashCycles 83547 # Number of cycles IEW is squashing (Cycle)

system.cpu.iew.blockCycles 89475 # Number of cycles IEW is blocking (Cycle)

system.cpu.iew.unblockCycles 15000856 # Number of cycles IEW is unblocking (Cycle)

system.cpu.iew.dispatchedInsts 77908902 # Number of instructions dispatched to IQ (Count)

system.cpu.iew.dispSquashedInsts 1 # Number of squashed instructions skipped by dispatch (Count)

system.cpu.iew.dispLoadInsts 15828722 # Number of dispatched load instructions (Count)

system.cpu.iew.dispStoreInsts 7414545 # Number of dispatched store instructions (Count)

system.cpu.iew.dispNonSpecInsts 34 # Number of dispatched non-speculative instructions (Count)

system.cpu.iew.iqFullEvents 7 # Number of times the IQ has become full, causing a stall (Count)

system.cpu.iew.lsqFullEvents 15000838 # Number of times the LSQ has become full, causing a stall (Count)

system.cpu.iew.memOrderViolationEvents 103 # Number of memory order violations (Count)

system.cpu.iew.predictedTakenIncorrect 77796 # Number of branches that were predicted taken incorrectly (Count)

system.cpu.iew.predictedNotTakenIncorrect 5677 # Number of branches that were predicted not taken incorrectly (Count)

system.cpu.iew.branchMispredicts 83473 # Number of branch mispredicts detected at execute (Count)

system.cpu.iew.instsToCommit 77147723 # Cumulative count of insts sent to commit (Count)

system.cpu.iew.writebackCount 77147572 # Cumulative count of insts written-back (Count)

system.cpu.iew.producerInst 54442198 # Number of instructions producing a value (Count)

system.cpu.iew.consumerInst 60991982 # Number of instructions consuming a value (Count)

system.cpu.iew.wbRate 0.155575 # Insts written-back per cycle ((Count/Cycle))

system.cpu.iew.wbFanout 0.892612 # Average fanout of values written-back ((Count/Count))

system.cpu.interrupts.clk\_domain.clock 16000 # Clock period in ticks (Tick)

system.cpu.lsq0.forwLoads 9324850 # Number of loads that had data forwarded from stores (Count)

system.cpu.lsq0.squashedLoads 254643 # Number of loads squashed (Count)

system.cpu.lsq0.ignoredResponses 0 # Number of memory responses ignored because the instruction is squashed (Count)

system.cpu.lsq0.memOrderViolation 103 # Number of memory ordering violations (Count)

system.cpu.lsq0.squashedStores 88739 # Number of stores squashed (Count)

system.cpu.lsq0.rescheduledLoads 0 # Number of loads that were rescheduled (Count)

system.cpu.lsq0.blockedByCache 2209889 # Number of times an access to memory failed due to the cache being blocked (Count)

system.cpu.lsq0.loadToUse::samples 15574079 # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::mean 25.365366 # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::stdev 37.482952 # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::0-9 9324215 59.87% 59.87% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::20-29 2122035 13.63% 73.50% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::50-59 871472 5.60% 79.09% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::60-69 60999 0.39% 79.48% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::70-79 225 0.00% 79.48% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::80-89 3010038 19.33% 98.81% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::90-99 82165 0.53% 99.34% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::100-109 390 0.00% 99.34% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::110-119 8 0.00% 99.34% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::120-129 345 0.00% 99.34% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::130-139 47522 0.31% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::140-149 36 0.00% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::150-159 1 0.00% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::170-179 1 0.00% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::180-189 6 0.00% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::190-199 1 0.00% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::220-229 6 0.00% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::230-239 34 0.00% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::240-249 106 0.00% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::250-259 528 0.00% 99.65% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::260-269 458 0.00% 99.66% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::270-279 656 0.00% 99.66% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::280-289 805 0.01% 99.67% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::290-299 657 0.00% 99.67% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::overflows 51370 0.33% 100.00% # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::min\_value 2 # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::max\_value 451 # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.lsq0.loadToUse::total 15574079 # Distribution of cycle latency between the first time a load is issued and its completion (Unspecified)

system.cpu.mmu.dtb.rdAccesses 15658795 # TLB accesses on read requests (Count)

system.cpu.mmu.dtb.wrAccesses 7326476 # TLB accesses on write requests (Count)

system.cpu.mmu.dtb.rdMisses 470 # TLB misses on read requests (Count)

system.cpu.mmu.dtb.wrMisses 28850 # TLB misses on write requests (Count)

system.cpu.mmu.dtb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 495887903000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.mmu.itb.rdAccesses 0 # TLB accesses on read requests (Count)

system.cpu.mmu.itb.wrAccesses 6497328 # TLB accesses on write requests (Count)

system.cpu.mmu.itb.rdMisses 0 # TLB misses on read requests (Count)

system.cpu.mmu.itb.wrMisses 93 # TLB misses on write requests (Count)

system.cpu.mmu.itb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 495887903000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.power\_state.pwrStateResidencyTicks::ON 495887903000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.rename.squashCycles 83547 # Number of cycles rename is squashing (Cycle)

system.cpu.rename.idleCycles 251062187 # Number of cycles rename is idle (Cycle)

system.cpu.rename.blockCycles 15090358 # Number of cycles rename is blocking (Cycle)

system.cpu.rename.serializeStallCycles 246 # count of cycles rename stalled for serializing inst (Cycle)

system.cpu.rename.runCycles 11956695 # Number of cycles rename is running (Cycle)

system.cpu.rename.unblockCycles 24335166 # Number of cycles rename is unblocking (Cycle)

system.cpu.rename.renamedInsts 77909147 # Number of instructions processed by rename (Count)

system.cpu.rename.ROBFullEvents 2 # Number of times rename has blocked due to ROB full (Count)

system.cpu.rename.IQFullEvents 236 # Number of times rename has blocked due to IQ full (Count)

system.cpu.rename.SQFullEvents 23668230 # Number of times rename has blocked due to SQ full (Count)

system.cpu.rename.renamedOperands 128819633 # Number of destination operands rename has renamed (Count)

system.cpu.rename.lookups 240155080 # Number of register rename lookups that rename has made (Count)

system.cpu.rename.intLookups 88369006 # Number of integer rename lookups (Count)

system.cpu.rename.fpLookups 1933 # Number of floating rename lookups (Count)

system.cpu.rename.committedMaps 126364676 # Number of HB maps that are committed (Count)

system.cpu.rename.undoneMaps 2454948 # Number of HB maps that are undone due to squashing (Count)

system.cpu.rename.serializing 8 # count of serializing insts renamed (Count)

system.cpu.rename.tempSerializing 8 # count of temporary serializing insts renamed (Count)

system.cpu.rename.skidInsts 12000898 # count of insts added to the skid buffer (Count)

system.cpu.rob.reads 380103226 # The number of ROB reads (Count)

system.cpu.rob.writes 155990359 # The number of ROB writes (Count)

system.cpu.thread\_0.numInsts 36199500 # Number of Instructions committed (Count)

system.cpu.thread\_0.numOps 76555494 # Number of Ops committed (Count)

system.cpu.thread\_0.numMemRefs 0 # Number of Memory References (Count)

system.cpu.workload.numSyscalls 17 # Number of system calls (Count)

system.mem\_ctrl.avgPriority\_cpu.inst::samples 6497296.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.avgPriority\_cpu.data::samples 4961408.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.priorityMinLatency 0.000000018750 # per QoS priority minimum request to response latency (Second)

system.mem\_ctrl.priorityMaxLatency 0.311197507750 # per QoS priority maximum request to response latency (Second)

system.mem\_ctrl.numReadWriteTurnArounds 46736 # Number of turnarounds from READ to WRITE (Count)

system.mem\_ctrl.numWriteReadTurnArounds 46736 # Number of turnarounds from WRITE to READ (Count)

system.mem\_ctrl.numStayReadState 26451082 # Number of times bus staying in READ state (Count)

system.mem\_ctrl.numStayWriteState 704929 # Number of times bus staying in WRITE state (Count)

system.mem\_ctrl.readReqs 12831113 # Number of read requests accepted (Count)

system.mem\_ctrl.writeReqs 7325807 # Number of write requests accepted (Count)

system.mem\_ctrl.readBursts 12831113 # Number of controller read bursts, including those serviced by the write queue (Count)

system.mem\_ctrl.writeBursts 7325807 # Number of controller write bursts, including those merged in the write queue (Count)

system.mem\_ctrl.servicedByWrQ 2122189 # Number of controller read bursts serviced by the write queue (Count)

system.mem\_ctrl.mergedWrBursts 6576027 # Number of controller write bursts merged with an existing one (Count)

system.mem\_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write (Count)

system.mem\_ctrl.avgRdQLen 2.07 # Average read queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.avgWrQLen 23.24 # Average write queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.numRdRetry 0 # Number of times read queue was full causing retry (Count)

system.mem\_ctrl.numWrRetry 0 # Number of times write queue was full causing retry (Count)

system.mem\_ctrl.readPktSize::0 1001314 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::1 24 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::2 5330404 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::3 2075 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::4 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::5 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::6 6497296 # Read request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::0 3122099 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::1 3 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::2 4201939 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::3 1766 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::4 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::5 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::6 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.rdQLenPdf::0 3203060 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::1 6518010 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::2 986402 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::3 734 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::4 278 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::5 155 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::6 98 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::7 67 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::8 33 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::9 25 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::10 24 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::11 20 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::12 6 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::13 4 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::14 3 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::15 2 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::16 1 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::17 1 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::18 1 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::0 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::1 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::2 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::3 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::4 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::5 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::6 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::7 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::8 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::9 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::10 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::11 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::12 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::13 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::14 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::15 909 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::16 944 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::17 20035 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::18 60717 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::19 47383 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::20 47351 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::21 47357 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::22 47372 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::23 47369 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::24 47293 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::25 47301 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::26 47364 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::27 47387 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::28 52355 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::29 48323 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::30 46785 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::31 46771 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::32 46749 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::34 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::35 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::50 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::51 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::53 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::54 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::55 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.rdPerTurnAround::samples 46736 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::mean 229.130863 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::stdev 20030.720262 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::0-262143 46735 100.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::4.1943e+06-4.45645e+06 1 0.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::total 46736 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.wrPerTurnAround::samples 46736 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::mean 16.042237 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::gmean 16.039588 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::stdev 0.304617 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::16 45827 98.06% 98.06% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::17 1 0.00% 98.06% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::18 752 1.61% 99.67% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::19 155 0.33% 100.00% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::20 1 0.00% 100.00% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::total 46736 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.bytesReadWrQ 135820096 # Total number of bytes read from write queue (Byte)

system.mem\_ctrl.bytesReadSys 438166513 # Total read bytes from the system interface side (Byte)

system.mem\_ctrl.bytesWrittenSys 19943987 # Total written bytes from the system interface side (Byte)

system.mem\_ctrl.avgRdBWSys 883599923.18667221 # Average system read bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.avgWrBWSys 40218740.72616770 # Average system write bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.totGap 495887893000 # Total gap between requests (Tick)

system.mem\_ctrl.avgGap 24601.37 # Average gap between requests ((Tick/Count))

system.mem\_ctrl.requestorReadBytes::cpu.inst 415826944 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorReadBytes::cpu.data 13849638 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorWriteBytes::cpu.data 878614 # Per-requestor bytes write to memory (Byte)

system.mem\_ctrl.requestorReadRate::cpu.inst 838550288.249318242073 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadRate::cpu.data 27928969.261426001787 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorWriteRate::cpu.data 1771799.623835550621 # Per-requestor bytes write to memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadAccesses::cpu.inst 6497296 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorReadAccesses::cpu.data 6333817 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorWriteAccesses::cpu.data 7325807 # Per-requestor write serviced memory accesses (Count)

system.mem\_ctrl.requestorReadTotalLat::cpu.inst 258411205000 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorReadTotalLat::cpu.data 202843452750 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorWriteTotalLat::cpu.data 11017646788500 # Per-requestor write total memory access latency (Tick)

system.mem\_ctrl.requestorReadAvgLat::cpu.inst 39772.12 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorReadAvgLat::cpu.data 32025.47 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorWriteAvgLat::cpu.data 1503949.91 # Per-requestor write average memory access latency ((Tick/Count))

system.mem\_ctrl.dram.bytesRead::cpu.inst 415826880 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::cpu.data 22339569 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::total 438166449 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::cpu.inst 415826880 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::total 415826880 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::cpu.data 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::total 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.numReads::cpu.inst 6497295 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::cpu.data 6333817 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::total 12831112 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::cpu.data 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::total 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.bwRead::cpu.inst 838550159 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::cpu.data 45049635 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::total 883599794 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::cpu.inst 838550159 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::total 838550159 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::cpu.data 40218741 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::total 40218741 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.inst 838550159 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.data 85268376 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::total 923818535 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.readBursts 10708924 # Number of DRAM read bursts (Count)

system.mem\_ctrl.dram.writeBursts 749750 # Number of DRAM write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::0 9761533 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::1 57754 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::2 58016 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::3 61829 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::4 65663 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::5 65660 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::6 65545 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::7 65696 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::8 65575 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::9 65929 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::10 65884 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::11 65592 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::12 65674 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::13 62819 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::14 57931 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::15 57824 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::0 83509 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::1 41674 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::2 41603 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::3 42298 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::4 44550 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::5 45300 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::6 45623 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::7 45935 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::8 46117 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::9 46320 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::10 46537 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::11 46733 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::12 46879 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::13 44948 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::14 40816 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::15 40908 # Per bank write bursts (Count)

system.mem\_ctrl.dram.totQLat 260462332750 # Total ticks spent queuing (Tick)

system.mem\_ctrl.dram.totBusLat 53544620000 # Total ticks spent in databus transfers (Tick)

system.mem\_ctrl.dram.totMemAccLat 461254657750 # Total ticks spent from burst creation until serviced by the DRAM (Tick)

system.mem\_ctrl.dram.avgQLat 24321.99 # Average queueing delay per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgBusLat 5000.00 # Average bus latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgMemAccLat 43071.99 # Average memory access latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.readRowHits 4119584 # Number of row buffer hits during reads (Count)

system.mem\_ctrl.dram.writeRowHits 688318 # Number of row buffer hits during writes (Count)

system.mem\_ctrl.dram.readRowHitRate 38.47 # Row buffer hit rate for reads (Ratio)

system.mem\_ctrl.dram.writeRowHitRate 91.81 # Row buffer hit rate for writes (Ratio)

system.mem\_ctrl.dram.bytesPerActivate::samples 6650760 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::mean 110.265683 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::gmean 93.794039 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::stdev 114.591988 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::0-127 3391789 51.00% 51.00% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::128-255 3143785 47.27% 98.27% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::256-383 8903 0.13% 98.40% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::384-511 4696 0.07% 98.47% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::512-639 3004 0.05% 98.52% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::640-767 3487 0.05% 98.57% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::768-895 5010 0.08% 98.65% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::896-1023 14191 0.21% 98.86% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::1024-1151 75895 1.14% 100.00% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::total 6650760 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesRead 685371136 # Total bytes read (Byte)

system.mem\_ctrl.dram.bytesWritten 47984000 # Total bytes written (Byte)

system.mem\_ctrl.dram.avgRdBW 1382.109005 # Average DRAM read bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.avgWrBW 96.763804 # Average DRAM write bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s ((Byte/Second))

system.mem\_ctrl.dram.busUtil 11.55 # Data bus utilization in percentage (Ratio)

system.mem\_ctrl.dram.busUtilRead 10.80 # Data bus utilization in percentage for reads (Ratio)

system.mem\_ctrl.dram.busUtilWrite 0.76 # Data bus utilization in percentage for writes (Ratio)

system.mem\_ctrl.dram.pageHitRate 41.96 # Row buffer hit rate, read and write combined (Ratio)

system.mem\_ctrl.dram.power\_state.pwrStateResidencyTicks::UNDEFINED 495887903000 # Cumulative time (in ticks) in various power states (Tick)

system.mem\_ctrl.dram.rank0.actEnergy 46995401460 # Energy for activate commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preEnergy 24978625485 # Energy for precharge commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.readEnergy 72840109440 # Energy for read commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.writeEnergy 2038368240 # Energy for write commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.refreshEnergy 39144577680.000008 # Energy for refresh commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actBackEnergy 178168711590 # Energy for active background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preBackEnergy 40384145280 # Energy for precharge background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.totalEnergy 404549939175 # Total energy per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.averagePower 815.809252 # Core power per rank (mW) (Watt)

system.mem\_ctrl.dram.rank0.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::IDLE 37382178500 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::REF 16558620000 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::SREF 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::PRE\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT 441947104500 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.actEnergy 491110620 # Energy for activate commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.preEnergy 261008715 # Energy for precharge commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.readEnergy 3621607920 # Energy for read commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.writeEnergy 1875326760 # Energy for write commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.refreshEnergy 39144577680.000008 # Energy for refresh commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.actBackEnergy 66463813740 # Energy for active background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.preBackEnergy 134451427680 # Energy for precharge background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.totalEnergy 246308873115 # Total energy per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.averagePower 496.702726 # Core power per rank (mW) (Watt)

system.mem\_ctrl.dram.rank1.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::IDLE 348505776500 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::REF 16558620000 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::SREF 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::PRE\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::ACT 130823506500 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::ACT\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.power\_state.pwrStateResidencyTicks::UNDEFINED 495887903000 # Cumulative time (in ticks) in various power states (Tick)

system.membus.transDist::ReadReq 12831097 # Transaction distribution (Count)

system.membus.transDist::ReadResp 12831096 # Transaction distribution (Count)

system.membus.transDist::WriteReq 7325791 # Transaction distribution (Count)

system.membus.transDist::WriteResp 7325791 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadResp 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteResp 16 # Transaction distribution (Count)

system.membus.pktCount\_system.cpu.icache\_port::system.mem\_ctrl.port 12994591 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.icache\_port::total 12994591 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::system.mem\_ctrl.port 27319248 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::total 27319248 # Packet count per connected requestor and responder (Count)

system.membus.pktCount::total 40313839 # Packet count per connected requestor and responder (Count)

system.membus.pktSize\_system.cpu.icache\_port::system.mem\_ctrl.port 415826880 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.icache\_port::total 415826880 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::system.mem\_ctrl.port 42283556 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::total 42283556 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize::total 458110436 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.snoops 0 # Total snoops (Count)

system.membus.snoopTraffic 0 # Total snoop traffic (Byte)

system.membus.snoopFanout::samples 20156920 # Request fanout histogram (Count)

system.membus.snoopFanout::mean 0 # Request fanout histogram (Count)

system.membus.snoopFanout::stdev 0 # Request fanout histogram (Count)

system.membus.snoopFanout::underflows 0 0.00% 0.00% # Request fanout histogram (Count)

system.membus.snoopFanout::0 20156920 100.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::1 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::overflows 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::min\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::max\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::total 20156920 # Request fanout histogram (Count)

system.membus.power\_state.pwrStateResidencyTicks::UNDEFINED 495887903000 # Cumulative time (in ticks) in various power states (Tick)

system.membus.reqLayer2.occupancy 27482727000 # Layer occupancy (ticks) (Tick)

system.membus.reqLayer2.utilization 0.1 # Layer utilization (Ratio)

system.membus.respLayer0.occupancy 34870803250 # Layer occupancy (ticks) (Tick)

system.membus.respLayer0.utilization 0.1 # Layer utilization (Ratio)

system.membus.respLayer1.occupancy 21328052248 # Layer occupancy (ticks) (Tick)

system.membus.respLayer1.utilization 0.0 # Layer utilization (Ratio)

system.membus.snoop\_filter.totRequests 0 # Total number of requests made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleRequests 0 # Number of requests hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiRequests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.membus.snoop\_filter.totSnoops 0 # Total number of snoops made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleSnoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiSnoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.workload.inst.arm 0 # number of arm instructions executed (Count)

system.workload.inst.quiesce 0 # number of quiesce instructions executed (Count)

---------- End Simulation Statistics ----------

**Stats 4.2**

---------- Begin Simulation Statistics ----------

simSeconds 2.904979 # Number of seconds simulated (Second)

simTicks 2904978744369 # Number of ticks simulated (Tick)

finalTick 2904978744369 # Number of ticks from beginning of simulation (restored from checkpoints and never reset) (Tick)

simFreq 1000000000000 # The number of ticks per simulated second ((Tick/Second))

hostSeconds 151.65 # Real time elapsed on the host (Second)

hostTickRate 19155619113 # The number of ticks simulated per host second (ticks/s) ((Tick/Second))

hostMemory 655496 # Number of bytes of host memory used (Byte)

simInsts 36199500 # Number of instructions simulated (Count)

simOps 76555494 # Number of ops (including micro ops) simulated (Count)

hostInstRate 238702 # Simulator instruction rate (inst/s) ((Count/Second))

hostOpRate 504812 # Simulator op (including micro ops) rate (op/s) ((Count/Second))

system.clk\_domain.clock 333 # Clock period in ticks (Tick)

system.clk\_domain.voltage\_domain.voltage 1 # Voltage in Volts (Volt)

system.cpu.numCycles 8723659893 # Number of cpu cycles simulated (Cycle)

system.cpu.numWorkItemsStarted 0 # Number of work items this cpu started (Count)

system.cpu.numWorkItemsCompleted 0 # Number of work items this cpu completed (Count)

system.cpu.exec\_context.thread\_0.numInsts 36199500 # Number of instructions committed (Count)

system.cpu.exec\_context.thread\_0.numOps 76555494 # Number of ops (including micro ops) committed (Count)

system.cpu.exec\_context.thread\_0.numIntAluAccesses 76554574 # Number of integer alu accesses (Count)

system.cpu.exec\_context.thread\_0.numFpAluAccesses 1471 # Number of float alu accesses (Count)

system.cpu.exec\_context.thread\_0.numVecAluAccesses 0 # Number of vector alu accesses (Count)

system.cpu.exec\_context.thread\_0.numCallsReturns 373 # Number of times a function call or return occured (Count)

system.cpu.exec\_context.thread\_0.numCondCtrlInsts 5125826 # Number of instructions that are conditional controls (Count)

system.cpu.exec\_context.thread\_0.numIntInsts 76554574 # Number of integer instructions (Count)

system.cpu.exec\_context.thread\_0.numFpInsts 1471 # Number of float instructions (Count)

system.cpu.exec\_context.thread\_0.numVecInsts 0 # Number of vector instructions (Count)

system.cpu.exec\_context.thread\_0.numIntRegReads 87007781 # Number of times the integer registers were read (Count)

system.cpu.exec\_context.thread\_0.numIntRegWrites 58976338 # Number of times the integer registers were written (Count)

system.cpu.exec\_context.thread\_0.numFpRegReads 1590 # Number of times the floating registers were read (Count)

system.cpu.exec\_context.thread\_0.numFpRegWrites 859 # Number of times the floating registers were written (Count)

system.cpu.exec\_context.thread\_0.numVecRegReads 0 # Number of times the vector registers were read (Count)

system.cpu.exec\_context.thread\_0.numVecRegWrites 0 # Number of times the vector registers were written (Count)

system.cpu.exec\_context.thread\_0.numVecPredRegReads 0 # Number of times the predicate registers were read (Count)

system.cpu.exec\_context.thread\_0.numVecPredRegWrites 0 # Number of times the predicate registers were written (Count)

system.cpu.exec\_context.thread\_0.numCCRegReads 26632889 # Number of times the CC registers were read (Count)

system.cpu.exec\_context.thread\_0.numCCRegWrites 24904504 # Number of times the CC registers were written (Count)

system.cpu.exec\_context.thread\_0.numMiscRegReads 37276209 # Number of times the Misc registers were read (Count)

system.cpu.exec\_context.thread\_0.numMiscRegWrites 0 # Number of times the Misc registers were written (Count)

system.cpu.exec\_context.thread\_0.numMemRefs 22899889 # Number of memory refs (Count)

system.cpu.exec\_context.thread\_0.numLoadInsts 15574080 # Number of load instructions (Count)

system.cpu.exec\_context.thread\_0.numStoreInsts 7325809 # Number of store instructions (Count)

system.cpu.exec\_context.thread\_0.numIdleCycles 0.003003 # Number of idle cycles (Cycle)

system.cpu.exec\_context.thread\_0.numBusyCycles 8723659892.996996 # Number of busy cycles (Cycle)

system.cpu.exec\_context.thread\_0.notIdleFraction 1.000000 # Percentage of non-idle cycles (Ratio)

system.cpu.exec\_context.thread\_0.idleFraction 0.000000 # Percentage of idle cycles (Ratio)

system.cpu.exec\_context.thread\_0.numBranches 5126544 # Number of branches fetched (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::No\_OpClass 236 0.00% 0.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntAlu 53654589 70.09% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntMult 177 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntDiv 28 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatAdd 184 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatCvt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMisc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAdd 8 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAddAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAlu 98 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdCvt 54 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMisc 252 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShift 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShiftAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatCvt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMisc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatReduceAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatReduceCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAes 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAesMix 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha1Hash 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha1Hash2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha256Hash 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha256Hash2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShaSigma2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShaSigma3 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdPredAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::MemRead 15573939 20.34% 90.43% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::MemWrite 7325245 9.57% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMemRead 141 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMemWrite 564 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IprAccess 0 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::InstPrefetch 0 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::total 76555515 # Class of executed instruction. (Count)

system.cpu.interrupts.clk\_domain.clock 5328 # Clock period in ticks (Tick)

system.cpu.mmu.dtb.rdAccesses 15574084 # TLB accesses on read requests (Count)

system.cpu.mmu.dtb.wrAccesses 7325810 # TLB accesses on write requests (Count)

system.cpu.mmu.dtb.rdMisses 421 # TLB misses on read requests (Count)

system.cpu.mmu.dtb.wrMisses 28844 # TLB misses on write requests (Count)

system.cpu.mmu.dtb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 2904978744369 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.mmu.itb.rdAccesses 0 # TLB accesses on read requests (Count)

system.cpu.mmu.itb.wrAccesses 47529643 # TLB accesses on write requests (Count)

system.cpu.mmu.itb.rdMisses 0 # TLB misses on read requests (Count)

system.cpu.mmu.itb.wrMisses 56 # TLB misses on write requests (Count)

system.cpu.mmu.itb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 2904978744369 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.power\_state.pwrStateResidencyTicks::ON 2904978744369 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.thread\_0.numInsts 0 # Number of Instructions committed (Count)

system.cpu.thread\_0.numOps 0 # Number of Ops committed (Count)

system.cpu.thread\_0.numMemRefs 0 # Number of Memory References (Count)

system.cpu.workload.numSyscalls 17 # Number of system calls (Count)

system.mem\_ctrl.avgPriority\_cpu.inst::samples 47529643.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.avgPriority\_cpu.data::samples 6943403.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.priorityMinLatency 0.000000018750 # per QoS priority minimum request to response latency (Second)

system.mem\_ctrl.priorityMaxLatency 1.983623239254 # per QoS priority maximum request to response latency (Second)

system.mem\_ctrl.numReadWriteTurnArounds 44371 # Number of turnarounds from READ to WRITE (Count)

system.mem\_ctrl.numWriteReadTurnArounds 44371 # Number of turnarounds from WRITE to READ (Count)

system.mem\_ctrl.numStayReadState 115552918 # Number of times bus staying in READ state (Count)

system.mem\_ctrl.numStayWriteState 666701 # Number of times bus staying in WRITE state (Count)

system.mem\_ctrl.readReqs 63103726 # Number of read requests accepted (Count)

system.mem\_ctrl.writeReqs 7325807 # Number of write requests accepted (Count)

system.mem\_ctrl.readBursts 63103726 # Number of controller read bursts, including those serviced by the write queue (Count)

system.mem\_ctrl.writeBursts 7325807 # Number of controller write bursts, including those merged in the write queue (Count)

system.mem\_ctrl.servicedByWrQ 9340636 # Number of controller read bursts serviced by the write queue (Count)

system.mem\_ctrl.mergedWrBursts 6615851 # Number of controller write bursts merged with an existing one (Count)

system.mem\_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write (Count)

system.mem\_ctrl.avgRdQLen 1.00 # Average read queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.avgWrQLen 24.97 # Average write queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.numRdRetry 0 # Number of times read queue was full causing retry (Count)

system.mem\_ctrl.numWrRetry 0 # Number of times write queue was full causing retry (Count)

system.mem\_ctrl.readPktSize::0 1001231 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::1 19 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::2 14571441 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::3 47531035 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::4 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::5 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::6 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::0 3122099 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::1 3 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::2 4201939 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::3 1766 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::4 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::5 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::6 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.rdQLenPdf::0 53763086 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::1 4 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::2 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::3 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::4 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::5 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::6 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::7 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::8 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::9 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::10 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::11 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::12 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::13 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::14 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::15 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::16 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::17 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::18 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::0 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::1 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::2 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::3 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::4 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::5 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::6 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::7 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::8 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::9 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::10 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::11 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::12 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::13 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::14 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::15 2 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::16 2 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::17 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::18 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::19 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::20 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::21 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::22 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::23 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::24 44372 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::25 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::26 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::27 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::28 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::29 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::30 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::31 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::32 44371 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::34 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::35 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::50 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::51 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::53 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::54 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::55 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.rdPerTurnAround::samples 44371 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::mean 1211.670122 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::gmean 338.242484 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::stdev 86586.289948 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::0-1.04858e+06 44370 100.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::1.78258e+07-1.88744e+07 1 0.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::total 44371 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.wrPerTurnAround::samples 44371 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::mean 16.000045 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::gmean 16.000042 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::stdev 0.009495 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::16 44370 100.00% 100.00% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::18 1 0.00% 100.00% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::total 44371 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.bytesReadWrQ 597800704 # Total number of bytes read from write queue (Byte)

system.mem\_ctrl.bytesReadSys 439535306 # Total read bytes from the system interface side (Byte)

system.mem\_ctrl.bytesWrittenSys 19943987 # Total written bytes from the system interface side (Byte)

system.mem\_ctrl.avgRdBWSys 151304138.40445256 # Average system read bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.avgWrBWSys 6865450.23389908 # Average system write bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.totGap 2904978632481 # Total gap between requests (Tick)

system.mem\_ctrl.avgGap 41246.60 # Average gap between requests ((Tick/Count))

system.mem\_ctrl.requestorReadBytes::cpu.inst 380237144 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorReadBytes::cpu.data 21934765 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorWriteBytes::cpu.data 721850 # Per-requestor bytes write to memory (Byte)

system.mem\_ctrl.requestorReadRate::cpu.inst 130891540.854489982128 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadRate::cpu.data 7550748.879838885739 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorWriteRate::cpu.data 248487.188210664666 # Per-requestor bytes write to memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadAccesses::cpu.inst 47529643 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorReadAccesses::cpu.data 15574083 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorWriteAccesses::cpu.data 7325807 # Per-requestor write serviced memory accesses (Count)

system.mem\_ctrl.requestorReadTotalLat::cpu.inst 1143607376552 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorReadTotalLat::cpu.data 267861554323 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorWriteTotalLat::cpu.data 70795069287956 # Per-requestor write total memory access latency (Tick)

system.mem\_ctrl.requestorReadAvgLat::cpu.inst 24060.93 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorReadAvgLat::cpu.data 17199.19 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorWriteAvgLat::cpu.data 9663791.21 # Per-requestor write average memory access latency ((Tick/Count))

system.mem\_ctrl.dram.bytesRead::cpu.inst 380237144 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::cpu.data 59298162 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::total 439535306 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::cpu.inst 380237144 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::total 380237144 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::cpu.data 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::total 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.numReads::cpu.inst 47529643 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::cpu.data 15574083 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::total 63103726 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::cpu.data 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::total 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.bwRead::cpu.inst 130891541 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::cpu.data 20412598 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::total 151304138 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::cpu.inst 130891541 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::total 130891541 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::cpu.data 6865450 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::total 6865450 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.inst 130891541 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.data 27278048 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::total 158169589 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.readBursts 53763090 # Number of DRAM read bursts (Count)

system.mem\_ctrl.dram.writeBursts 709938 # Number of DRAM write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::0 52805285 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::1 58690 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::2 58157 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::3 61971 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::4 66160 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::5 66349 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::6 65557 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::7 66179 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::8 65688 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::9 67381 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::10 66785 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::11 65843 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::12 66137 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::13 62865 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::14 58979 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::15 61064 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::0 44533 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::1 41907 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::2 41515 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::3 42093 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::4 44340 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::5 45115 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::6 45484 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::7 45866 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::8 46100 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::9 46302 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::10 46512 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::11 46708 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::12 46858 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::13 44924 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::14 40794 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::15 40887 # Per bank write bursts (Count)

system.mem\_ctrl.dram.totQLat 403410993375 # Total ticks spent queuing (Tick)

system.mem\_ctrl.dram.totBusLat 268815450000 # Total ticks spent in databus transfers (Tick)

system.mem\_ctrl.dram.totMemAccLat 1411468930875 # Total ticks spent from burst creation until serviced by the DRAM (Tick)

system.mem\_ctrl.dram.avgQLat 7503.49 # Average queueing delay per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgBusLat 5000.00 # Average bus latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgMemAccLat 26253.49 # Average memory access latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.readRowHits 42188256 # Number of row buffer hits during reads (Count)

system.mem\_ctrl.dram.writeRowHits 648271 # Number of row buffer hits during writes (Count)

system.mem\_ctrl.dram.readRowHitRate 78.47 # Row buffer hit rate for reads (Ratio)

system.mem\_ctrl.dram.writeRowHitRate 91.31 # Row buffer hit rate for writes (Ratio)

system.mem\_ctrl.dram.bytesPerActivate::samples 11636492 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::mean 299.597937 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::gmean 170.594697 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::stdev 305.879668 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::0-127 5442191 46.77% 46.77% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::128-255 2170999 18.66% 65.43% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::256-383 68240 0.59% 66.01% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::384-511 243053 2.09% 68.10% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::512-639 993233 8.54% 76.64% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::640-767 2082764 17.90% 94.53% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::768-895 3089 0.03% 94.56% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::896-1023 3745 0.03% 94.59% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::1024-1151 629178 5.41% 100.00% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::total 11636492 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesRead 3440837760 # Total bytes read (Byte)

system.mem\_ctrl.dram.bytesWritten 45436032 # Total bytes written (Byte)

system.mem\_ctrl.dram.avgRdBW 1184.462285 # Average DRAM read bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.avgWrBW 15.640745 # Average DRAM write bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s ((Byte/Second))

system.mem\_ctrl.dram.busUtil 9.38 # Data bus utilization in percentage (Ratio)

system.mem\_ctrl.dram.busUtilRead 9.25 # Data bus utilization in percentage for reads (Ratio)

system.mem\_ctrl.dram.busUtilWrite 0.12 # Data bus utilization in percentage for writes (Ratio)

system.mem\_ctrl.dram.pageHitRate 78.64 # Row buffer hit rate, read and write combined (Ratio)

system.mem\_ctrl.dram.power\_state.pwrStateResidencyTicks::UNDEFINED 2904978744369 # Cumulative time (in ticks) in various power states (Tick)

system.mem\_ctrl.dram.rank0.actEnergy 82411657860 # Energy for activate commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preEnergy 43802815980 # Energy for precharge commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.readEnergy 380193204720 # Energy for read commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.writeEnergy 1831452660 # Energy for write commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.refreshEnergy 229316037600.000031 # Energy for refresh commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actBackEnergy 1259461453290 # Energy for active background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preBackEnergy 54912719520 # Energy for precharge background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.totalEnergy 2051929341630 # Total energy per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.averagePower 706.349176 # Core power per rank (mW) (Watt)

system.mem\_ctrl.dram.rank0.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::IDLE 16427461440 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::REF 97003400000 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::SREF 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::PRE\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT 2791547882929 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.actEnergy 672959280 # Energy for activate commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.preEnergy 357671160 # Energy for precharge commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.readEnergy 3675257880 # Energy for read commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.writeEnergy 1874423700 # Energy for write commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.refreshEnergy 229316037600.000031 # Energy for refresh commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.actBackEnergy 261012021960 # Energy for active background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.preBackEnergy 895712240640 # Energy for precharge background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.totalEnergy 1392620612220 # Total energy per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.averagePower 479.390982 # Core power per rank (mW) (Watt)

system.mem\_ctrl.dram.rank1.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::IDLE 2326194428411 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::REF 97003400000 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::SREF 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::PRE\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::ACT 481780915958 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::ACT\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.power\_state.pwrStateResidencyTicks::UNDEFINED 2904978744369 # Cumulative time (in ticks) in various power states (Tick)

system.membus.transDist::ReadReq 63103710 # Transaction distribution (Count)

system.membus.transDist::ReadResp 63103710 # Transaction distribution (Count)

system.membus.transDist::WriteReq 7325791 # Transaction distribution (Count)

system.membus.transDist::WriteResp 7325791 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadResp 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteResp 16 # Transaction distribution (Count)

system.membus.pktCount\_system.cpu.icache\_port::system.mem\_ctrl.port 95059286 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.icache\_port::total 95059286 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::system.mem\_ctrl.port 45799780 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::total 45799780 # Packet count per connected requestor and responder (Count)

system.membus.pktCount::total 140859066 # Packet count per connected requestor and responder (Count)

system.membus.pktSize\_system.cpu.icache\_port::system.mem\_ctrl.port 380237144 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.icache\_port::total 380237144 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::system.mem\_ctrl.port 79242149 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::total 79242149 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize::total 459479293 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.snoops 0 # Total snoops (Count)

system.membus.snoopTraffic 0 # Total snoop traffic (Byte)

system.membus.snoopFanout::samples 70429533 # Request fanout histogram (Count)

system.membus.snoopFanout::mean 0 # Request fanout histogram (Count)

system.membus.snoopFanout::stdev 0 # Request fanout histogram (Count)

system.membus.snoopFanout::underflows 0 0.00% 0.00% # Request fanout histogram (Count)

system.membus.snoopFanout::0 70429533 100.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::1 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::overflows 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::min\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::max\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::total 70429533 # Request fanout histogram (Count)

system.membus.power\_state.pwrStateResidencyTicks::UNDEFINED 2904978744369 # Cumulative time (in ticks) in various power states (Tick)

system.membus.reqLayer2.occupancy 25892528220 # Layer occupancy (ticks) (Tick)

system.membus.reqLayer2.utilization 0.0 # Layer utilization (Ratio)

system.membus.respLayer0.occupancy 40605288314 # Layer occupancy (ticks) (Tick)

system.membus.respLayer0.utilization 0.0 # Layer utilization (Ratio)

system.membus.respLayer1.occupancy 18475240264 # Layer occupancy (ticks) (Tick)

system.membus.respLayer1.utilization 0.0 # Layer utilization (Ratio)

system.membus.snoop\_filter.totRequests 0 # Total number of requests made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleRequests 0 # Number of requests hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiRequests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.membus.snoop\_filter.totSnoops 0 # Total number of snoops made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleSnoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiSnoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.workload.inst.arm 0 # number of arm instructions executed (Count)

system.workload.inst.quiesce 0 # number of quiesce instructions executed (Count)

---------- End Simulation Statistics ----------

**Stats 4.3**

---------- Begin Simulation Statistics ----------

simSeconds 3.271749 # Number of seconds simulated (Second)

simTicks 3271748533000 # Number of ticks simulated (Tick)

finalTick 3271748533000 # Number of ticks from beginning of simulation (restored from checkpoints and never reset) (Tick)

simFreq 1000000000000 # The number of ticks per simulated second ((Tick/Second))

hostSeconds 152.52 # Real time elapsed on the host (Second)

hostTickRate 21450822174 # The number of ticks simulated per host second (ticks/s) ((Tick/Second))

hostMemory 655496 # Number of bytes of host memory used (Byte)

simInsts 36199500 # Number of instructions simulated (Count)

simOps 76555494 # Number of ops (including micro ops) simulated (Count)

hostInstRate 237337 # Simulator instruction rate (inst/s) ((Count/Second))

hostOpRate 501926 # Simulator op (including micro ops) rate (op/s) ((Count/Second))

system.clk\_domain.clock 1000 # Clock period in ticks (Tick)

system.clk\_domain.voltage\_domain.voltage 1 # Voltage in Volts (Volt)

system.cpu.numCycles 3271748533 # Number of cpu cycles simulated (Cycle)

system.cpu.numWorkItemsStarted 0 # Number of work items this cpu started (Count)

system.cpu.numWorkItemsCompleted 0 # Number of work items this cpu completed (Count)

system.cpu.exec\_context.thread\_0.numInsts 36199500 # Number of instructions committed (Count)

system.cpu.exec\_context.thread\_0.numOps 76555494 # Number of ops (including micro ops) committed (Count)

system.cpu.exec\_context.thread\_0.numIntAluAccesses 76554574 # Number of integer alu accesses (Count)

system.cpu.exec\_context.thread\_0.numFpAluAccesses 1471 # Number of float alu accesses (Count)

system.cpu.exec\_context.thread\_0.numVecAluAccesses 0 # Number of vector alu accesses (Count)

system.cpu.exec\_context.thread\_0.numCallsReturns 373 # Number of times a function call or return occured (Count)

system.cpu.exec\_context.thread\_0.numCondCtrlInsts 5125826 # Number of instructions that are conditional controls (Count)

system.cpu.exec\_context.thread\_0.numIntInsts 76554574 # Number of integer instructions (Count)

system.cpu.exec\_context.thread\_0.numFpInsts 1471 # Number of float instructions (Count)

system.cpu.exec\_context.thread\_0.numVecInsts 0 # Number of vector instructions (Count)

system.cpu.exec\_context.thread\_0.numIntRegReads 87007781 # Number of times the integer registers were read (Count)

system.cpu.exec\_context.thread\_0.numIntRegWrites 58976338 # Number of times the integer registers were written (Count)

system.cpu.exec\_context.thread\_0.numFpRegReads 1590 # Number of times the floating registers were read (Count)

system.cpu.exec\_context.thread\_0.numFpRegWrites 859 # Number of times the floating registers were written (Count)

system.cpu.exec\_context.thread\_0.numVecRegReads 0 # Number of times the vector registers were read (Count)

system.cpu.exec\_context.thread\_0.numVecRegWrites 0 # Number of times the vector registers were written (Count)

system.cpu.exec\_context.thread\_0.numVecPredRegReads 0 # Number of times the predicate registers were read (Count)

system.cpu.exec\_context.thread\_0.numVecPredRegWrites 0 # Number of times the predicate registers were written (Count)

system.cpu.exec\_context.thread\_0.numCCRegReads 26632889 # Number of times the CC registers were read (Count)

system.cpu.exec\_context.thread\_0.numCCRegWrites 24904504 # Number of times the CC registers were written (Count)

system.cpu.exec\_context.thread\_0.numMiscRegReads 37276209 # Number of times the Misc registers were read (Count)

system.cpu.exec\_context.thread\_0.numMiscRegWrites 0 # Number of times the Misc registers were written (Count)

system.cpu.exec\_context.thread\_0.numMemRefs 22899889 # Number of memory refs (Count)

system.cpu.exec\_context.thread\_0.numLoadInsts 15574080 # Number of load instructions (Count)

system.cpu.exec\_context.thread\_0.numStoreInsts 7325809 # Number of store instructions (Count)

system.cpu.exec\_context.thread\_0.numIdleCycles 0.001000 # Number of idle cycles (Cycle)

system.cpu.exec\_context.thread\_0.numBusyCycles 3271748532.999000 # Number of busy cycles (Cycle)

system.cpu.exec\_context.thread\_0.notIdleFraction 1.000000 # Percentage of non-idle cycles (Ratio)

system.cpu.exec\_context.thread\_0.idleFraction 0.000000 # Percentage of idle cycles (Ratio)

system.cpu.exec\_context.thread\_0.numBranches 5126544 # Number of branches fetched (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::No\_OpClass 236 0.00% 0.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntAlu 53654589 70.09% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntMult 177 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntDiv 28 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatAdd 184 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatCvt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMisc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAdd 8 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAddAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAlu 98 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdCvt 54 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMisc 252 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShift 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShiftAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatCvt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMisc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatReduceAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatReduceCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAes 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAesMix 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha1Hash 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha1Hash2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha256Hash 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha256Hash2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShaSigma2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShaSigma3 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdPredAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::MemRead 15573939 20.34% 90.43% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::MemWrite 7325245 9.57% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMemRead 141 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMemWrite 564 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IprAccess 0 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::InstPrefetch 0 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::total 76555515 # Class of executed instruction. (Count)

system.cpu.interrupts.clk\_domain.clock 16000 # Clock period in ticks (Tick)

system.cpu.mmu.dtb.rdAccesses 15574084 # TLB accesses on read requests (Count)

system.cpu.mmu.dtb.wrAccesses 7325810 # TLB accesses on write requests (Count)

system.cpu.mmu.dtb.rdMisses 421 # TLB misses on read requests (Count)

system.cpu.mmu.dtb.wrMisses 28844 # TLB misses on write requests (Count)

system.cpu.mmu.dtb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 3271748533000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.mmu.itb.rdAccesses 0 # TLB accesses on read requests (Count)

system.cpu.mmu.itb.wrAccesses 47529643 # TLB accesses on write requests (Count)

system.cpu.mmu.itb.rdMisses 0 # TLB misses on read requests (Count)

system.cpu.mmu.itb.wrMisses 56 # TLB misses on write requests (Count)

system.cpu.mmu.itb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 3271748533000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.power\_state.pwrStateResidencyTicks::ON 3271748533000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.thread\_0.numInsts 0 # Number of Instructions committed (Count)

system.cpu.thread\_0.numOps 0 # Number of Ops committed (Count)

system.cpu.thread\_0.numMemRefs 0 # Number of Memory References (Count)

system.cpu.workload.numSyscalls 17 # Number of system calls (Count)

system.mem\_ctrl.avgPriority\_cpu.inst::samples 47529643.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.avgPriority\_cpu.data::samples 6926926.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.priorityMinLatency 0.000000016842 # per QoS priority minimum request to response latency (Second)

system.mem\_ctrl.priorityMaxLatency 2.172427269932 # per QoS priority maximum request to response latency (Second)

system.mem\_ctrl.numReadWriteTurnArounds 44297 # Number of turnarounds from READ to WRITE (Count)

system.mem\_ctrl.numWriteReadTurnArounds 44297 # Number of turnarounds from WRITE to READ (Count)

system.mem\_ctrl.numStayReadState 115615734 # Number of times bus staying in READ state (Count)

system.mem\_ctrl.numStayWriteState 665331 # Number of times bus staying in WRITE state (Count)

system.mem\_ctrl.readReqs 63103726 # Number of read requests accepted (Count)

system.mem\_ctrl.writeReqs 7325807 # Number of write requests accepted (Count)

system.mem\_ctrl.readBursts 63103726 # Number of controller read bursts, including those serviced by the write queue (Count)

system.mem\_ctrl.writeBursts 7325807 # Number of controller write bursts, including those merged in the write queue (Count)

system.mem\_ctrl.servicedByWrQ 9356785 # Number of controller read bursts serviced by the write queue (Count)

system.mem\_ctrl.mergedWrBursts 6616179 # Number of controller write bursts merged with an existing one (Count)

system.mem\_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write (Count)

system.mem\_ctrl.avgRdQLen 1.00 # Average read queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.avgWrQLen 26.95 # Average write queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.numRdRetry 0 # Number of times read queue was full causing retry (Count)

system.mem\_ctrl.numWrRetry 0 # Number of times write queue was full causing retry (Count)

system.mem\_ctrl.readPktSize::0 1001231 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::1 19 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::2 14571441 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::3 47531035 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::4 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::5 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::6 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::0 3122099 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::1 3 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::2 4201939 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::3 1766 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::4 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::5 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::6 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.rdQLenPdf::0 53746937 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::1 4 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::2 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::3 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::4 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::5 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::6 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::7 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::8 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::9 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::10 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::11 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::12 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::13 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::14 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::15 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::16 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::17 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::18 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::0 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::1 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::2 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::3 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::4 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::5 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::6 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::7 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::8 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::9 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::10 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::11 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::12 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::13 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::14 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::15 428 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::16 428 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::17 44298 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::18 44298 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::19 44298 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::20 44298 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::21 44298 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::22 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::23 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::24 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::25 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::26 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::27 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::28 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::29 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::30 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::31 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::32 44297 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::34 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::35 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::50 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::51 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::53 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::54 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::55 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.rdPerTurnAround::samples 44297 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::mean 1213.325440 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::gmean 338.733664 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::stdev 86658.496903 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::0-1.04858e+06 44296 100.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::1.78258e+07-1.88744e+07 1 0.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::total 44297 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.wrPerTurnAround::samples 44297 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::mean 16.019279 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::gmean 16.018176 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::stdev 0.195415 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::16 43870 99.04% 99.04% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::18 427 0.96% 100.00% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::total 44297 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.bytesReadWrQ 598834240 # Total number of bytes read from write queue (Byte)

system.mem\_ctrl.bytesReadSys 439535306 # Total read bytes from the system interface side (Byte)

system.mem\_ctrl.bytesWrittenSys 19943987 # Total written bytes from the system interface side (Byte)

system.mem\_ctrl.avgRdBWSys 134342631.03251770 # Average system read bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.avgWrBWSys 6095819.03952519 # Average system write bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.totGap 3271748412000 # Total gap between requests (Tick)

system.mem\_ctrl.avgGap 46454.21 # Average gap between requests ((Tick/Count))

system.mem\_ctrl.requestorReadBytes::cpu.inst 380237144 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorReadBytes::cpu.data 21870171 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorWriteBytes::cpu.data 719938 # Per-requestor bytes write to memory (Byte)

system.mem\_ctrl.requestorReadRate::cpu.inst 116218327.956685915589 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadRate::cpu.data 6684551.327649361454 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorWriteRate::cpu.data 220046.862629708106 # Per-requestor bytes write to memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadAccesses::cpu.inst 47529643 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorReadAccesses::cpu.data 15574083 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorWriteAccesses::cpu.data 7325807 # Per-requestor write serviced memory accesses (Count)

system.mem\_ctrl.requestorReadTotalLat::cpu.inst 1046412273808 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorReadTotalLat::cpu.data 254768310736 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorWriteTotalLat::cpu.data 85141809253008 # Per-requestor write total memory access latency (Tick)

system.mem\_ctrl.requestorReadAvgLat::cpu.inst 22015.99 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorReadAvgLat::cpu.data 16358.48 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorWriteAvgLat::cpu.data 11622174.77 # Per-requestor write average memory access latency ((Tick/Count))

system.mem\_ctrl.dram.bytesRead::cpu.inst 380237144 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::cpu.data 59298162 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::total 439535306 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::cpu.inst 380237144 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::total 380237144 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::cpu.data 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::total 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.numReads::cpu.inst 47529643 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::cpu.data 15574083 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::total 63103726 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::cpu.data 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::total 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.bwRead::cpu.inst 116218328 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::cpu.data 18124303 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::total 134342631 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::cpu.inst 116218328 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::total 116218328 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::cpu.data 6095819 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::total 6095819 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.inst 116218328 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.data 24220122 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::total 140438450 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.readBursts 53746941 # Number of DRAM read bursts (Count)

system.mem\_ctrl.dram.writeBursts 709606 # Number of DRAM write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::0 52789130 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::1 58693 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::2 58167 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::3 61969 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::4 66160 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::5 66349 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::6 65557 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::7 66179 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::8 65688 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::9 67381 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::10 66785 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::11 65848 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::12 66124 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::13 62866 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::14 58981 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::15 61064 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::0 44015 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::1 41937 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::2 41594 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::3 42161 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::4 44341 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::5 45114 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::6 45486 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::7 45865 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::8 46102 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::9 46303 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::10 46513 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::11 46708 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::12 46857 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::13 44926 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::14 40796 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::15 40888 # Per bank write bursts (Count)

system.mem\_ctrl.dram.totQLat 395974604222 # Total ticks spent queuing (Tick)

system.mem\_ctrl.dram.totBusLat 201658522632 # Total ticks spent in databus transfers (Tick)

system.mem\_ctrl.dram.totMemAccLat 1301180584544 # Total ticks spent from burst creation until serviced by the DRAM (Tick)

system.mem\_ctrl.dram.avgQLat 7367.39 # Average queueing delay per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgBusLat 3752.00 # Average bus latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgMemAccLat 24209.39 # Average memory access latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.readRowHits 42113187 # Number of row buffer hits during reads (Count)

system.mem\_ctrl.dram.writeRowHits 648956 # Number of row buffer hits during writes (Count)

system.mem\_ctrl.dram.readRowHitRate 78.35 # Row buffer hit rate for reads (Ratio)

system.mem\_ctrl.dram.writeRowHitRate 91.45 # Row buffer hit rate for writes (Ratio)

system.mem\_ctrl.dram.bytesPerActivate::samples 11694403 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::mean 298.024518 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::gmean 169.571890 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::stdev 306.218865 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::0-127 5464845 46.73% 46.73% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::128-255 2236969 19.13% 65.86% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::256-383 86170 0.74% 66.60% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::384-511 251437 2.15% 68.75% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::512-639 938593 8.03% 76.77% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::640-767 2061445 17.63% 94.40% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::768-895 3086 0.03% 94.43% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::896-1023 3723 0.03% 94.46% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::1024-1151 648135 5.54% 100.00% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::total 11694403 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesRead 3439804224 # Total bytes read (Byte)

system.mem\_ctrl.dram.bytesWritten 45414784 # Total bytes written (Byte)

system.mem\_ctrl.dram.avgRdBW 1051.365711 # Average DRAM read bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.avgWrBW 13.880891 # Average DRAM write bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.peakBW 17057.00 # Theoretical peak bandwidth in MiByte/s ((Byte/Second))

system.mem\_ctrl.dram.busUtil 6.25 # Data bus utilization in percentage (Ratio)

system.mem\_ctrl.dram.busUtilRead 6.16 # Data bus utilization in percentage for reads (Ratio)

system.mem\_ctrl.dram.busUtilWrite 0.08 # Data bus utilization in percentage for writes (Ratio)

system.mem\_ctrl.dram.pageHitRate 78.53 # Row buffer hit rate, read and write combined (Ratio)

system.mem\_ctrl.dram.power\_state.pwrStateResidencyTicks::UNDEFINED 3271748533000 # Cumulative time (in ticks) in various power states (Tick)

system.mem\_ctrl.dram.rank0.actEnergy 122155663279.023529 # Energy for activate commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preEnergy 60294777315.755035 # Energy for precharge commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.readEnergy 352318832675.713135 # Energy for read commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.writeEnergy 1783309196.255445 # Energy for write commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.refreshEnergy 270838752737.947968 # Energy for refresh commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actBackEnergy 1651197300621.838623 # Energy for active background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preBackEnergy 64149527831.815384 # Energy for precharge background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.totalEnergy 2522738163657.621582 # Total energy per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.averagePower 771.067256 # Core power per rank (mW) (Watt)

system.mem\_ctrl.dram.rank0.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::IDLE 22855615048 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::REF 109241600000 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::SREF 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::PRE\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT 3139651317952 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.actEnergy 1052086613.762582 # Energy for activate commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.preEnergy 519299161.921046 # Energy for precharge commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.readEnergy 3406801247.139291 # Energy for read commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.writeEnergy 1826961765.215440 # Energy for write commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.refreshEnergy 270838752737.947968 # Energy for refresh commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.actBackEnergy 329616363731.653137 # Energy for active background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.preBackEnergy 1175478952037.081787 # Energy for precharge background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.totalEnergy 1782739217290.326904 # Total energy per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank1.averagePower 544.888826 # Core power per rank (mW) (Watt)

system.mem\_ctrl.dram.rank1.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::IDLE 2641049451722 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::REF 109241600000 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::SREF 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::PRE\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::ACT 521457481278 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank1.pwrStateTime::ACT\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.power\_state.pwrStateResidencyTicks::UNDEFINED 3271748533000 # Cumulative time (in ticks) in various power states (Tick)

system.membus.transDist::ReadReq 63103710 # Transaction distribution (Count)

system.membus.transDist::ReadResp 63103710 # Transaction distribution (Count)

system.membus.transDist::WriteReq 7325791 # Transaction distribution (Count)

system.membus.transDist::WriteResp 7325791 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadResp 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteResp 16 # Transaction distribution (Count)

system.membus.pktCount\_system.cpu.icache\_port::system.mem\_ctrl.port 95059286 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.icache\_port::total 95059286 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::system.mem\_ctrl.port 45799780 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::total 45799780 # Packet count per connected requestor and responder (Count)

system.membus.pktCount::total 140859066 # Packet count per connected requestor and responder (Count)

system.membus.pktSize\_system.cpu.icache\_port::system.mem\_ctrl.port 380237144 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.icache\_port::total 380237144 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::system.mem\_ctrl.port 79242149 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::total 79242149 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize::total 459479293 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.snoops 0 # Total snoops (Count)

system.membus.snoopTraffic 0 # Total snoop traffic (Byte)

system.membus.snoopFanout::samples 70429533 # Request fanout histogram (Count)

system.membus.snoopFanout::mean 0 # Request fanout histogram (Count)

system.membus.snoopFanout::stdev 0 # Request fanout histogram (Count)

system.membus.snoopFanout::underflows 0 0.00% 0.00% # Request fanout histogram (Count)

system.membus.snoopFanout::0 70429533 100.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::1 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::overflows 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::min\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::max\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::total 70429533 # Request fanout histogram (Count)

system.membus.power\_state.pwrStateResidencyTicks::UNDEFINED 3271748533000 # Cumulative time (in ticks) in various power states (Tick)

system.membus.reqLayer2.occupancy 77755340000 # Layer occupancy (ticks) (Tick)

system.membus.reqLayer2.utilization 0.0 # Layer utilization (Ratio)

system.membus.respLayer0.occupancy 106964241192 # Layer occupancy (ticks) (Tick)

system.membus.respLayer0.utilization 0.0 # Layer utilization (Ratio)

system.membus.respLayer1.occupancy 43751319264 # Layer occupancy (ticks) (Tick)

system.membus.respLayer1.utilization 0.0 # Layer utilization (Ratio)

system.membus.snoop\_filter.totRequests 0 # Total number of requests made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleRequests 0 # Number of requests hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiRequests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.membus.snoop\_filter.totSnoops 0 # Total number of snoops made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleSnoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiSnoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.workload.inst.arm 0 # number of arm instructions executed (Count)

system.workload.inst.quiesce 0 # number of quiesce instructions executed (Count)

---------- End Simulation Statistics ----------

**Stats 4.4**

---------- Begin Simulation Statistics ----------

simSeconds 3.387931 # Number of seconds simulated (Second)

simTicks 3387931467000 # Number of ticks simulated (Tick)

finalTick 3387931467000 # Number of ticks from beginning of simulation (restored from checkpoints and never reset) (Tick)

simFreq 1000000000000 # The number of ticks per simulated second ((Tick/Second))

hostSeconds 147.19 # Real time elapsed on the host (Second)

hostTickRate 23017532962 # The number of ticks simulated per host second (ticks/s) ((Tick/Second))

hostMemory 655500 # Number of bytes of host memory used (Byte)

simInsts 36199500 # Number of instructions simulated (Count)

simOps 76555494 # Number of ops (including micro ops) simulated (Count)

hostInstRate 245938 # Simulator instruction rate (inst/s) ((Count/Second))

hostOpRate 520116 # Simulator op (including micro ops) rate (op/s) ((Count/Second))

system.clk\_domain.clock 1000 # Clock period in ticks (Tick)

system.clk\_domain.voltage\_domain.voltage 1 # Voltage in Volts (Volt)

system.cpu.numCycles 3387931467 # Number of cpu cycles simulated (Cycle)

system.cpu.numWorkItemsStarted 0 # Number of work items this cpu started (Count)

system.cpu.numWorkItemsCompleted 0 # Number of work items this cpu completed (Count)

system.cpu.exec\_context.thread\_0.numInsts 36199500 # Number of instructions committed (Count)

system.cpu.exec\_context.thread\_0.numOps 76555494 # Number of ops (including micro ops) committed (Count)

system.cpu.exec\_context.thread\_0.numIntAluAccesses 76554574 # Number of integer alu accesses (Count)

system.cpu.exec\_context.thread\_0.numFpAluAccesses 1471 # Number of float alu accesses (Count)

system.cpu.exec\_context.thread\_0.numVecAluAccesses 0 # Number of vector alu accesses (Count)

system.cpu.exec\_context.thread\_0.numCallsReturns 373 # Number of times a function call or return occured (Count)

system.cpu.exec\_context.thread\_0.numCondCtrlInsts 5125826 # Number of instructions that are conditional controls (Count)

system.cpu.exec\_context.thread\_0.numIntInsts 76554574 # Number of integer instructions (Count)

system.cpu.exec\_context.thread\_0.numFpInsts 1471 # Number of float instructions (Count)

system.cpu.exec\_context.thread\_0.numVecInsts 0 # Number of vector instructions (Count)

system.cpu.exec\_context.thread\_0.numIntRegReads 87007781 # Number of times the integer registers were read (Count)

system.cpu.exec\_context.thread\_0.numIntRegWrites 58976338 # Number of times the integer registers were written (Count)

system.cpu.exec\_context.thread\_0.numFpRegReads 1590 # Number of times the floating registers were read (Count)

system.cpu.exec\_context.thread\_0.numFpRegWrites 859 # Number of times the floating registers were written (Count)

system.cpu.exec\_context.thread\_0.numVecRegReads 0 # Number of times the vector registers were read (Count)

system.cpu.exec\_context.thread\_0.numVecRegWrites 0 # Number of times the vector registers were written (Count)

system.cpu.exec\_context.thread\_0.numVecPredRegReads 0 # Number of times the predicate registers were read (Count)

system.cpu.exec\_context.thread\_0.numVecPredRegWrites 0 # Number of times the predicate registers were written (Count)

system.cpu.exec\_context.thread\_0.numCCRegReads 26632889 # Number of times the CC registers were read (Count)

system.cpu.exec\_context.thread\_0.numCCRegWrites 24904504 # Number of times the CC registers were written (Count)

system.cpu.exec\_context.thread\_0.numMiscRegReads 37276209 # Number of times the Misc registers were read (Count)

system.cpu.exec\_context.thread\_0.numMiscRegWrites 0 # Number of times the Misc registers were written (Count)

system.cpu.exec\_context.thread\_0.numMemRefs 22899889 # Number of memory refs (Count)

system.cpu.exec\_context.thread\_0.numLoadInsts 15574080 # Number of load instructions (Count)

system.cpu.exec\_context.thread\_0.numStoreInsts 7325809 # Number of store instructions (Count)

system.cpu.exec\_context.thread\_0.numIdleCycles 0.001000 # Number of idle cycles (Cycle)

system.cpu.exec\_context.thread\_0.numBusyCycles 3387931466.999000 # Number of busy cycles (Cycle)

system.cpu.exec\_context.thread\_0.notIdleFraction 1.000000 # Percentage of non-idle cycles (Ratio)

system.cpu.exec\_context.thread\_0.idleFraction 0.000000 # Percentage of idle cycles (Ratio)

system.cpu.exec\_context.thread\_0.numBranches 5126544 # Number of branches fetched (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::No\_OpClass 236 0.00% 0.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntAlu 53654589 70.09% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntMult 177 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IntDiv 28 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatAdd 184 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatCvt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMisc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAdd 8 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAddAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAlu 98 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdCvt 54 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMisc 252 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShift 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShiftAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatCvt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatDiv 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMisc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMult 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatMultAcc 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatSqrt 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdReduceCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatReduceAdd 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdFloatReduceCmp 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAes 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdAesMix 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha1Hash 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha1Hash2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha256Hash 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdSha256Hash2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShaSigma2 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdShaSigma3 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::SimdPredAlu 0 0.00% 70.09% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::MemRead 15573939 20.34% 90.43% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::MemWrite 7325245 9.57% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMemRead 141 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::FloatMemWrite 564 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::IprAccess 0 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::InstPrefetch 0 0.00% 100.00% # Class of executed instruction. (Count)

system.cpu.exec\_context.thread\_0.statExecutedInstType::total 76555515 # Class of executed instruction. (Count)

system.cpu.interrupts.clk\_domain.clock 16000 # Clock period in ticks (Tick)

system.cpu.mmu.dtb.rdAccesses 15574084 # TLB accesses on read requests (Count)

system.cpu.mmu.dtb.wrAccesses 7325810 # TLB accesses on write requests (Count)

system.cpu.mmu.dtb.rdMisses 421 # TLB misses on read requests (Count)

system.cpu.mmu.dtb.wrMisses 28844 # TLB misses on write requests (Count)

system.cpu.mmu.dtb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 3387931467000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.mmu.itb.rdAccesses 0 # TLB accesses on read requests (Count)

system.cpu.mmu.itb.wrAccesses 47529643 # TLB accesses on write requests (Count)

system.cpu.mmu.itb.rdMisses 0 # TLB misses on read requests (Count)

system.cpu.mmu.itb.wrMisses 56 # TLB misses on write requests (Count)

system.cpu.mmu.itb.walker.power\_state.pwrStateResidencyTicks::UNDEFINED 3387931467000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.power\_state.pwrStateResidencyTicks::ON 3387931467000 # Cumulative time (in ticks) in various power states (Tick)

system.cpu.thread\_0.numInsts 0 # Number of Instructions committed (Count)

system.cpu.thread\_0.numOps 0 # Number of Ops committed (Count)

system.cpu.thread\_0.numMemRefs 0 # Number of Memory References (Count)

system.cpu.workload.numSyscalls 17 # Number of system calls (Count)

system.mem\_ctrl.avgPriority\_cpu.inst::samples 47529643.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.avgPriority\_cpu.data::samples 7256330.00 # Average QoS priority value for accepted requests (Count)

system.mem\_ctrl.priorityMinLatency 0.000000022500 # per QoS priority minimum request to response latency (Second)

system.mem\_ctrl.priorityMaxLatency 2.128645477500 # per QoS priority maximum request to response latency (Second)

system.mem\_ctrl.numReadWriteTurnArounds 62023 # Number of turnarounds from READ to WRITE (Count)

system.mem\_ctrl.numWriteReadTurnArounds 62023 # Number of turnarounds from WRITE to READ (Count)

system.mem\_ctrl.numStayReadState 115720873 # Number of times bus staying in READ state (Count)

system.mem\_ctrl.numStayWriteState 932486 # Number of times bus staying in WRITE state (Count)

system.mem\_ctrl.readReqs 63103726 # Number of read requests accepted (Count)

system.mem\_ctrl.writeReqs 7325807 # Number of write requests accepted (Count)

system.mem\_ctrl.readBursts 63103730 # Number of controller read bursts, including those serviced by the write queue (Count)

system.mem\_ctrl.writeBursts 7325807 # Number of controller write bursts, including those merged in the write queue (Count)

system.mem\_ctrl.servicedByWrQ 9310160 # Number of controller read bursts serviced by the write queue (Count)

system.mem\_ctrl.mergedWrBursts 6333404 # Number of controller write bursts merged with an existing one (Count)

system.mem\_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write (Count)

system.mem\_ctrl.avgRdQLen 1.00 # Average read queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.avgWrQLen 26.46 # Average write queue length when enqueuing ((Count/Tick))

system.mem\_ctrl.numRdRetry 0 # Number of times read queue was full causing retry (Count)

system.mem\_ctrl.numWrRetry 0 # Number of times write queue was full causing retry (Count)

system.mem\_ctrl.readPktSize::0 1001233 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::1 19 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::2 14571444 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::3 47531034 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::4 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::5 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.readPktSize::6 0 # Read request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::0 3122099 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::1 3 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::2 4201939 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::3 1766 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::4 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::5 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.writePktSize::6 0 # Write request sizes (log2) (Count)

system.mem\_ctrl.rdQLenPdf::0 53793562 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::1 8 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::2 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::3 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::4 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::5 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::6 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::7 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::8 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::9 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::10 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::11 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::12 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::13 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::14 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::15 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::16 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::17 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::18 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::0 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::1 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::2 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::3 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::4 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::5 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::6 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::7 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::8 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::9 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::10 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::11 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::12 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::13 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::14 1 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::15 2 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::16 2 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::17 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::18 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::19 62025 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::20 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::21 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::22 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::23 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::24 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::25 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::26 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::27 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::28 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::29 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::30 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::31 62024 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::32 62023 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::34 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::35 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::50 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::51 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::53 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::54 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::55 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see (Count)

system.mem\_ctrl.rdPerTurnAround::samples 62023 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::mean 867.307160 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::gmean 304.355664 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::stdev 73227.667422 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::0-1.04858e+06 62022 100.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::1.78258e+07-1.88744e+07 1 0.00% 100.00% # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.rdPerTurnAround::total 62023 # Reads before turning the bus around for writes (Count)

system.mem\_ctrl.wrPerTurnAround::samples 62023 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::mean 16.000048 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::gmean 16.000044 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::stdev 0.012046 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::16 62022 100.00% 100.00% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::19 1 0.00% 100.00% # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.wrPerTurnAround::total 62023 # Writes before turning the bus around for reads (Count)

system.mem\_ctrl.bytesReadWrQ 297925120 # Total number of bytes read from write queue (Byte)

system.mem\_ctrl.bytesReadSys 439535306 # Total read bytes from the system interface side (Byte)

system.mem\_ctrl.bytesWrittenSys 19943987 # Total written bytes from the system interface side (Byte)

system.mem\_ctrl.avgRdBWSys 129735595.38652852 # Average system read bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.avgWrBWSys 5886774.03727423 # Average system write bandwidth in Byte/s ((Byte/Second))

system.mem\_ctrl.totGap 3387931331000 # Total gap between requests (Tick)

system.mem\_ctrl.avgGap 48103.84 # Average gap between requests ((Tick/Count))

system.mem\_ctrl.requestorReadBytes::cpu.inst 380237144 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorReadBytes::cpu.data 22056285 # Per-requestor bytes read from memory (Byte)

system.mem\_ctrl.requestorWriteBytes::cpu.data 1163629 # Per-requestor bytes write to memory (Byte)

system.mem\_ctrl.requestorReadRate::cpu.inst 112232832.246957615018 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadRate::cpu.data 6510251.229943194427 # Per-requestor bytes read from memory rate ((Byte/Second))

system.mem\_ctrl.requestorWriteRate::cpu.data 343462.968874747923 # Per-requestor bytes write to memory rate ((Byte/Second))

system.mem\_ctrl.requestorReadAccesses::cpu.inst 47529643 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorReadAccesses::cpu.data 15574087 # Per-requestor read serviced memory accesses (Count)

system.mem\_ctrl.requestorWriteAccesses::cpu.data 7325807 # Per-requestor write serviced memory accesses (Count)

system.mem\_ctrl.requestorReadTotalLat::cpu.inst 1224887811000 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorReadTotalLat::cpu.data 182313768000 # Per-requestor read total memory access latency (Tick)

system.mem\_ctrl.requestorWriteTotalLat::cpu.data 88885120788000 # Per-requestor write total memory access latency (Tick)

system.mem\_ctrl.requestorReadAvgLat::cpu.inst 25771.03 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorReadAvgLat::cpu.data 11706.23 # Per-requestor read average memory access latency ((Tick/Count))

system.mem\_ctrl.requestorWriteAvgLat::cpu.data 12133150.76 # Per-requestor write average memory access latency ((Tick/Count))

system.mem\_ctrl.dram.bytesRead::cpu.inst 380237144 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::cpu.data 59298162 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesRead::total 439535306 # Number of bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::cpu.inst 380237144 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesInstRead::total 380237144 # Number of instructions bytes read from this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::cpu.data 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.bytesWritten::total 19943987 # Number of bytes written to this memory (Byte)

system.mem\_ctrl.dram.numReads::cpu.inst 47529643 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::cpu.data 15574083 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numReads::total 63103726 # Number of read requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::cpu.data 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.numWrites::total 7325807 # Number of write requests responded to by this memory (Count)

system.mem\_ctrl.dram.bwRead::cpu.inst 112232832 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::cpu.data 17502763 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwRead::total 129735595 # Total read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::cpu.inst 112232832 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwInstRead::total 112232832 # Instruction read bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::cpu.data 5886774 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwWrite::total 5886774 # Write bandwidth from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.inst 112232832 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::cpu.data 23389537 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.bwTotal::total 135622369 # Total bandwidth to/from this memory ((Byte/Second))

system.mem\_ctrl.dram.readBursts 53793570 # Number of DRAM read bursts (Count)

system.mem\_ctrl.dram.writeBursts 992371 # Number of DRAM write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::0 126621 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::1 126555 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::2 127943 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::3 126552 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::4 126701 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::5 40486923 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::6 7284384 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankRdBursts::7 5387891 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::0 118186 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::1 116867 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::2 116664 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::3 116551 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::4 116808 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::5 116455 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::6 118233 # Per bank write bursts (Count)

system.mem\_ctrl.dram.perBankWrBursts::7 172607 # Per bank write bursts (Count)

system.mem\_ctrl.dram.totQLat 196846254000 # Total ticks spent queuing (Tick)

system.mem\_ctrl.dram.totBusLat 403451775000 # Total ticks spent in databus transfers (Tick)

system.mem\_ctrl.dram.totMemAccLat 1407201579000 # Total ticks spent from burst creation until serviced by the DRAM (Tick)

system.mem\_ctrl.dram.avgQLat 3659.29 # Average queueing delay per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgBusLat 7500.00 # Average bus latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.avgMemAccLat 26159.29 # Average memory access latency per DRAM burst ((Tick/Count))

system.mem\_ctrl.dram.readRowHits 48755173 # Number of row buffer hits during reads (Count)

system.mem\_ctrl.dram.writeRowHits 813478 # Number of row buffer hits during writes (Count)

system.mem\_ctrl.dram.readRowHitRate 90.63 # Row buffer hit rate for reads (Ratio)

system.mem\_ctrl.dram.writeRowHitRate 81.97 # Row buffer hit rate for writes (Ratio)

system.mem\_ctrl.dram.bytesPerActivate::samples 5217285 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::mean 336.027119 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::gmean 262.139173 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::stdev 176.764011 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::0-63 454273 8.71% 8.71% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::64-127 291986 5.60% 14.30% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::128-191 629921 12.07% 26.38% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::192-255 679885 13.03% 39.41% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::256-319 166639 3.19% 42.60% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::320-383 478304 9.17% 51.77% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::384-447 230113 4.41% 56.18% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::448-511 25557 0.49% 56.67% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::512-575 2260607 43.33% 100.00% # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesPerActivate::total 5217285 # Bytes accessed per row activation (Byte)

system.mem\_ctrl.dram.bytesRead 1721394240 # Total bytes read (Byte)

system.mem\_ctrl.dram.bytesWritten 31755872 # Total bytes written (Byte)

system.mem\_ctrl.dram.avgRdBW 508.095945 # Average DRAM read bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.avgWrBW 9.373233 # Average DRAM write bandwidth in MiBytes/s ((Byte/Second))

system.mem\_ctrl.dram.peakBW 4266.00 # Theoretical peak bandwidth in MiByte/s ((Byte/Second))

system.mem\_ctrl.dram.busUtil 12.13 # Data bus utilization in percentage (Ratio)

system.mem\_ctrl.dram.busUtilRead 11.91 # Data bus utilization in percentage for reads (Ratio)

system.mem\_ctrl.dram.busUtilWrite 0.22 # Data bus utilization in percentage for writes (Ratio)

system.mem\_ctrl.dram.pageHitRate 90.48 # Row buffer hit rate, read and write combined (Ratio)

system.mem\_ctrl.dram.power\_state.pwrStateResidencyTicks::UNDEFINED 3387931467000 # Cumulative time (in ticks) in various power states (Tick)

system.mem\_ctrl.dram.rank0.actEnergy 15870651838.931707 # Energy for activate commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preEnergy 5590692348.189857 # Energy for precharge commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.readEnergy 92399364690.435654 # Energy for read commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.writeEnergy 1530307532.710258 # Energy for write commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.refreshEnergy 24220584765.927349 # Energy for refresh commands per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actBackEnergy 135013861347.384048 # Energy for active background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.preBackEnergy 2148532790.391415 # Energy for precharge background per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.totalEnergy 276773995313.910522 # Total energy per rank (pJ) (Joule)

system.mem\_ctrl.dram.rank0.averagePower 81.694095 # Core power per rank (mW) (Watt)

system.mem\_ctrl.dram.rank0.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::IDLE 21526133500 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::REF 113367020000 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::SREF 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::PRE\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT 3253038313500 # Time in different power states (Tick)

system.mem\_ctrl.dram.rank0.pwrStateTime::ACT\_PDN 0 # Time in different power states (Tick)

system.mem\_ctrl.power\_state.pwrStateResidencyTicks::UNDEFINED 3387931467000 # Cumulative time (in ticks) in various power states (Tick)

system.membus.transDist::ReadReq 63103710 # Transaction distribution (Count)

system.membus.transDist::ReadResp 63103710 # Transaction distribution (Count)

system.membus.transDist::WriteReq 7325791 # Transaction distribution (Count)

system.membus.transDist::WriteResp 7325791 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWReadResp 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteReq 16 # Transaction distribution (Count)

system.membus.transDist::LockedRMWWriteResp 16 # Transaction distribution (Count)

system.membus.pktCount\_system.cpu.icache\_port::system.mem\_ctrl.port 95059286 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.icache\_port::total 95059286 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::system.mem\_ctrl.port 45799780 # Packet count per connected requestor and responder (Count)

system.membus.pktCount\_system.cpu.dcache\_port::total 45799780 # Packet count per connected requestor and responder (Count)

system.membus.pktCount::total 140859066 # Packet count per connected requestor and responder (Count)

system.membus.pktSize\_system.cpu.icache\_port::system.mem\_ctrl.port 380237144 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.icache\_port::total 380237144 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::system.mem\_ctrl.port 79242149 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize\_system.cpu.dcache\_port::total 79242149 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.pktSize::total 459479293 # Cumulative packet size per connected requestor and responder (Byte)

system.membus.snoops 0 # Total snoops (Count)

system.membus.snoopTraffic 0 # Total snoop traffic (Byte)

system.membus.snoopFanout::samples 70429533 # Request fanout histogram (Count)

system.membus.snoopFanout::mean 0 # Request fanout histogram (Count)

system.membus.snoopFanout::stdev 0 # Request fanout histogram (Count)

system.membus.snoopFanout::underflows 0 0.00% 0.00% # Request fanout histogram (Count)

system.membus.snoopFanout::0 70429533 100.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::1 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::overflows 0 0.00% 100.00% # Request fanout histogram (Count)

system.membus.snoopFanout::min\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::max\_value 0 # Request fanout histogram (Count)

system.membus.snoopFanout::total 70429533 # Request fanout histogram (Count)

system.membus.power\_state.pwrStateResidencyTicks::UNDEFINED 3387931467000 # Cumulative time (in ticks) in various power states (Tick)

system.membus.reqLayer2.occupancy 77755340000 # Layer occupancy (ticks) (Tick)

system.membus.reqLayer2.utilization 0.0 # Layer utilization (Ratio)

system.membus.respLayer0.occupancy 118807065000 # Layer occupancy (ticks) (Tick)

system.membus.respLayer0.utilization 0.0 # Layer utilization (Ratio)

system.membus.respLayer1.occupancy 41604287000 # Layer occupancy (ticks) (Tick)

system.membus.respLayer1.utilization 0.0 # Layer utilization (Ratio)

system.membus.snoop\_filter.totRequests 0 # Total number of requests made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleRequests 0 # Number of requests hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiRequests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.membus.snoop\_filter.totSnoops 0 # Total number of snoops made to the snoop filter. (Count)

system.membus.snoop\_filter.hitSingleSnoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data. (Count)

system.membus.snoop\_filter.hitMultiSnoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)

system.workload.inst.arm 0 # number of arm instructions executed (Count)

system.workload.inst.quiesce 0 # number of quiesce instructions executed (Count)

---------- End Simulation Statistics ----------